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# AN IMPROVED APPROACH TO TRACE ROUTINES

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**GODDARD SPACE FLIGHT CENTER**  
**GREENBELT, MARYLAND**

AN IMPROVED APPROACH TO TRACE ROUTINES

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## PART 1

### AN IMPROVED APPROACH TO TRACE ROUTINES

#### INTRODUCTION

Analyzing the flow of executed computer programs is among the most fundamental and essential techniques of debugging. With increasing sophistication in both computer hardware and software determining program flow is becoming progressively more difficult. Complicating factors are address indexing, indirect addressing, automatic allocation of relocatable subroutines, a wealth of resident monitor and library routines, chaining, and both manual and automatic overlay facilities.

The classic approach to unwinding these factors and presenting useful diagnostic information to the program has been and will continue to be — at least for the foreseeable future — the use of trace programs. Through the use of hardware interrupts and interpretive software routines, changes in sequential addressing of computer programs by jumps (branches) and tests (compares) can be detected, interpreted, and reported to the programmer.

#### Problems

Despite the value of trace routines, several serious drawbacks have deterred programmers from their use. Perhaps the worst of these are considerably extended execution time and overabundance of printed diagnostic material. Among the secondary problems is the inability of users to provide "own-coding" subroutines for extended usage.

This document proposes a solution to these problems. It also describes usage of the trace routine embodying these improvements for the Univac 1107.

#### Option Control

Increasing the speed and efficiency of trace programs can be approached on two fronts: first, application of utmost skill and ingenuity in developing the routine; second, allowing flexible control of option-subroutines to eliminate unwanted processing. The former approach will not be discussed because it is ultimately limited by hardware; the latter approach however, is limited only by imagination.

When developing a routine, a systems analyst first asks, "What should it do?" Partial answers come from the historic solutions to similar problems; further answers are obtained by polling likely users of the routine for recommendations. Generally, the analyst cannot obtain agreement without devising a system encompassing all options. Such a task is burdensome not only to the developer, but to the user as well. Furthermore, it defies speed and efficiency.

Enigmatically a solution to option control is to eliminate all but one option: that is, to allow the use of arbitrary externally defined subroutines which are callable by the trace routine. For discussion purposes, such a subroutine will be termed a subservient.

The trace routine can be written to leave the same basic information available to all subservients. Normally this will be the origin and destination addresses representing a change in sequential addressing, and will be called a FROM-TO address pair. In this manner all subservients can be independent. It is now possible to construct a basic set of subservients, each performing a unique function. In addition, any subservient can be called by another, so that a composite of functions can be selected to fulfill a required task.

The advantage of this procedure from a user's standpoint is that he himself can select a subservient for his problem. In the simplest case, he can request a single subservient made available on a standard library; in this instance, no coding is required. In a more advanced situation, he may wish to construct his own subservient, consisting of imbedded calls to any number of library subservients. Thus, only those required components are executed. Also, no option-testing logic is necessary, as the user has coded these options into his own subservient.

#### Minimization of Printing

When using most print options in a trace program, the user often finds himself surrounded with paper. Also, it is likely that exaggerated execution time or high print load has prevented him from reaching the conditions he wants traced. Even if these conditions were encountered, mechanical problems of shuffling paper may discourage him from further pursuits. Circumstances such as these often cause a trace routine to be relegated to a position of secondary importance.

An initial step to an effective solution is to eliminate printing for all but the most essential information, the FROM-TO address pairs. Such a decision is not too severe because the ability to construct and nest subservients allows the user to reconstruct reports of more exacting information. Also, as will be favored by some computer installations, this approach places the heaviest burden on those programmers requiring the most demanding printouts, but does not penalize the average user. Unfortunately, adoption of this initial step is not entirely adequate in resolving the problem of sheer paper volume.

If it were possible, the most desirable solution would be to avoid printing completely. Perhaps the next best alternative is to retain trace information in a core table for selective printing at the end of the job. In reality, however, few tables would be extensive enough to retain significant data; core would speedily become exhausted.

Despite apparent problems development of an adequate core table is still practicable. By storing cyclically in the table — overlaying from top to bottom — a fixed amount of data is maintained. In addition, only the most recent address pairs are left available because predecessors for each position in the table have been overstored. This constant updating will continue until tracing is terminated by user request, normal end of job, or abnormal end of job. The import of this data at abnormal completion is obvious.

To help offset limitations imposed by a cyclic table, options can be provided which allow the user to establish the length of this table. Also, enhancements can be provided for efficient use of the table: for example, a repeat count for iterated address pairs can optimize storage by compressing the data.

Finally, it is necessary to print the table. As this now occurs after program execution, various post mortem routines are usually available in utility packages to provide this core dump. Characteristically, such routines maximize output on the printed line, provide reasonable options for format control, and operate efficiently. A combination like this is usually more than adequate for programmer needs.

#### Extended Usage

Knowing all subservients are furnished with the same FROM-TO address pair information, the user can code and nest virtually any special trace techniques he desires. A variety of library and resident monitor subroutines is generally available to assist him. Among the most significant applications for the trace routine described in Section II are:

1. Dynamic dumping of arbitrarily selected memory locations at the time of each traced instruction
2. Continuous testing for jumps (branches) to illegal destinations, and execution of an error routine for these events
3. Continuous testing to detect which instruction or I/O operation is over-storing specific cells in memory, and execution of an error routine for these events

4. Computation of the distribution of operation codes in an executing program, including - at the user's discretion - library and resident monitor routines
5. Continuous detection and logging of points where characteristic overflow, characteristic underflow, divide overflow, occur
6. Various combinations of the above practices

Note that no modifications, other than a call to the trace routine, are needed to apply these techniques to existing programs.

## PART II

### A TRACE ROUTINE FOR THE UNIVAC 1107

#### INTRODUCTION

The trace routine is a blend between a software and hardware trace. Software components are necessary to allow for restoring register R3 after a trace interrupt occurs. They also permit establishing the locations of all executed JMGI/MOJP (not provided by a trace interrupt) and of all instructions performing a skip. Hardware components of this routine are used solely for detecting that a jump instruction was executed, for obtaining the address to which control was to be transferred, and for returning control to the trace routine.

#### Sleuth II Calling Sequences

In general, the SLEUTH II calling sequence for initiating trace is:

LMJ	11, TRC\$
+	interrupt routine entry point, mode
+	lower core limit, upper core limit
+	address of trace storage table, length of table (dependent)

Parameters are interpreted as follows:

Mode:	value 0 means trace jumps only
	value 1 means trace jumps and skips only
	value 2 means trace all instructions

Interrupt routine entry point: Starting line of routine to which control is transferred after detecting a condition determined by the selected mode. Upon entry to this routine, A0 will contain the address of the jump or skip; A1 will contain the address for the next sequential instruction. Entry to the interrupt routine is made by an SLJ instruction.

Upper and lower core limits: Core limits in which the trace is permitted to report to the interrupt routine.

Address of trace storage table, length of table: These parameters are needed only when using standard interrupt routines described later. These routines develop tables of trace information in user-defined core regions.



All tracing is terminated by the calling sequence

LMJ        11, TRCX\$

Re-entry without reinitialization to the last trace function is by

LMJ        11, TRCR\$

The procedures equivalent to these calls are:

T\$RC        interrupt routine entry point, mode                                ;  
             lower core limit, upper core limit                                ;  
             address of trace storage table, length of table  
T\$RCX  
T\$RCR

#### The General Interrupt Routine Facility

By supplying a label to his own routine, the user can process all traced instructions that occur with either the FROM or TO address in his designated core limits. These addresses are available to him in A0 and A1 respectively. (The contents of A0 and A1 before trace interrupt occurred may be found in cells TRCA0\$ and TRCA1\$) If registers other than A0 and A1 are used in the interrupt routine, they must be saved and restored by the user before returning control. Entry to the interrupt routine is made by an SLJ instruction.

The calling sequence for this routine is:

LMJ        11, TRC\$  
+        routine name, tract mode of 0, 1, or 2  
+        lower core limit, upper core limit  
or  
T\$RC        routine name, mode    ;  
             lower core limit, upper core limit

#### The TRCY\$ Standard Interrupt Routine

This routine stores information into a user-specified storage table. Storage is made cyclically; that is, once the area is filled, overlaying will occur from the top. A single negative zero is placed after the last written value to signal a division between the old area and the new.

When either the traced FROM address or TO address is within the designated core limits, an address pair in the format +(FROM, TO) is inserted in

the table. However, if this address pair is identical to the previous pair, a repeat count, N, is developed and stored instead. This is identified by the format (-Ø, N).

If a call to TRCY\$ is made via T\$RC from within the designated core area, the address pair +(address of call, address of next sequential instruction) is generated.

The calling sequence for this routine is:

LMJ	11, TRC\$
+TRCY\$,	trace mode of Ø, 1, or 2
+	lower core limit, upper core limit
+	storage table address, table length
or	
T\$RC	TRCY\$, mode      lower core limit, upper core limit      ;
	storage table address, table length

#### The TRCP\$ Standard Interrupt Routine

This routine sets a one-bit in the user's storage table to show a traced instruction in the designated core area was executed. The table is constructed so that each bit of a 36-bit word represents an address relative to the lower core limit address. If the indicated table length is exceeded, no storage will occur but the trace will be continued.

If a call to TRCP\$ via T\$RC is made from within the designated core area, a one-bit corresponding to the linkage address is set.

The calling sequence for this routine is:

LMJ	11, TRC\$
+TRCP\$,	trace mode of Ø, 1 or 2
+	lower core limit, upper core limit
+	storage table address, table length
or	
T\$RC	TRCP\$, mode      lower core limit, upper core limit      ;
	storage table address, table length

#### Nested Calls to Interrupt Routines

It is possible to define a general interrupt routine which can make use of the TRCY\$ and TRCP\$ routines. The following techniques must be used:

1. Before using TRCY\$ or TRCP\$, registers A0 and A1 should contain the values of the FROM and TO addresses supplied to the general interrupt routine by the trace program. Calls to the standard interrupt routines are made by SLJ TRCP\$ or SLJ TRCY\$. Registers A0 and A1 are altered before return from these calls.
2. Before initiating the trace routine, the required routines TRCY\$ or TRCP\$ must be initialized by making T\$RC calls with the desired standard and the general interrupt routine names. The mode and the lower and upper core limits must be identical in all calls. Furthermore, the linkage initiating the general interrupt routine must be made last.

### Example of Nested Interrupt Routine Usage

Problem: Find the origin of a jump to location 0. Take the MERR\$ exit if the instruction is executed. In the continued process of testing, record trace information with both TRCY\$ and TRCP\$.

Sample

```
Solution: T$RC    TRCY$,1    0100000,010440    ;
              CYBIN, 1000
           T$RC    TRCP$,1    0100000,010440    ;
              PBIN, 8
           T$RC    UTRACE,1    0100000,010440
              .
              .
              .
```

```
UTRACE J        $
      JZ        13,MERR$ . TO address = 0, FROM in A0
      S         12, SAVE12
      S         13, SAVE13
      SLJ       TRCY$
      L         12, SAVE12
      L         13, SAVE13
      SLJ       TRCP$
      J         UTRACE . return to trace routine
SAVE12 +0
SAVE13 +0
CYBIN  RES      1000
PBIN   RES      8
```

Description: The first linkage initializes TRCY\$ to store FROM-TO address pairs cyclically in table CYBIN. Only 1000 address pairs will be

retained. The second linkage initializes TRCP\$. The eight cells of 36 bits each in table PBIN is sufficient to contain all information for the designated core limits. The third linkage establishes the user-defined routine UTRACE. Since it is the last called, it takes precedence over the previous calls without disrupting initialization of TRCY\$ and TRCP\$.

At the interrupt for each traced jump instruction, the trace routine leaves the origin address of the jump in A0 and the destination address in A1. An SLJ to the users UTRACE is made. The user tests against A1 to see if it is zero. If so, the MERR\$ exit is taken. A0 is unchanged and can be found in the automatic MERR\$ thin-film dump. If A1 is non-zero, the user first saves A0 and A1 from future destruction by TRCY\$. He calls TRCY\$ and then restores A0 and A1 before calling TRCP\$. There is no need to restore A0 and A1 before returning to the main trace program.

#### FORTTRAN IV Calling Sequences

In general all trace-initiating calling sequences are in the form:

CALL NTRC (I, M, \$X, \$Y, BIN, L)

All FORIV trace routines are terminated by:

CALL NTRCX

All fields of NTRC must be provided. They are interpreted as follows: (the mnemonics used are not relevant).

Field I - a numeric value    1 identifies TRCY\$  
                                  2 identifies TRCP\$

Field M - a numeric value    0 traces jumps only  
                                  1 traces jumps and skips only  
                                  2 traces all instructions

Field \$X - the statement number corresponding to the lower core limit

Field \$Y - the statement number corresponding to the upper core limit

Field BIN - name of the array where storage will occur

Field L - the number of cells available in this array for storage

#### Action Taken on Incorrect Parameters

There is one error condition for which corrective actions are made and parameter interpretation continued. If the low core limit and upper core limit

are reversed, these are shifted. For all other parameter errors, the designated trace routine is not initiated. Instead the console message:

"\*\*\*(N)TRC(\$) CALL ERROR FROM XXXXXX"

is typed, and control is restored to the calling program.

The following list summarizes these remaining error conditions:

1. Specified core limits do not encompass a portion of core memory 000000-017777.
2. Storage table start location is not in core.
3. Last address of core storage table exceeds location 017777.
4. The label identifying the interrupt routine entry point is undefined.
5. An illegal mode was specified.
6. Re-entry was attempted without prior use of the trace routine.

#### Trace Limitations

The limitations listed here, which may appear imposing, are normally quite remote from the mainstream of normal programs. Most references are to I/O interrupts which at worst only reduce the effectiveness of trace and do not introduce error conditions. The restrictions are:

1. Trace may not be initiated with interrupts disabled (i.e., usually during coding) unless the first instruction below the linkage is a PAIJ I/O interrupt. Without this instruction, the trace routine assumes that interrupts may be allowed and initially performs a AAIJ. No special coding is required to initiate the trace during "main-line coding".
2. The interrupt "location" MITRC\$ is used by the trace. Any attempts to change MITRC\$ will allow the change, terminate the trace, and return control to the main program without introducing errors. Such a condition results when an unsolicited "E" key-in or MERR\$, MXXX\$, MEXIT\$ (or monitor equivalent) exit occurs.
3. The trace routine will not trace I/O interrupts. The real-time clock interrupt is in this class. However, once the interrupt has been processed, the trace will resume at the interrupted instruction.

4. All I/O interrupts which interrupt the trace routine must restore control with interrupts allowed. (All monitor resident and library routines are written in this manner.)
5. Jumps to the trace routine which are themselves traced will first turn off the trace before being executed. Subsequent logic depends on the entry point.
6. The trace routine is vulnerable to being overwritten by erroneous programs. However, it cannot be overlaid by a MAP because it resides in independent core.
7. All registers other than A0 and A1 used in the general interrupt routine must be saved and restored before re-entry to the trace routine.
8. The address saved in parking register R3 after a traced repeated sequence will be the location of an execute remote instruction in the trace routine itself.
9. If an error interrupt occurs, the address of the offending instruction will be the same location mentioned in item 8 only if the interrupt location contains an EX instruction ultimately referencing an LMJ or SLJ.
10. If an error interrupt location contains an PAIJ or an EX ultimately referencing it, interrupts are prevented belatedly (that is, interrupts are allowed first by the trace routine but prevented before the next main program instruction is executed).
11. Error interrupt locations containing jumps must not require indirect addressing, B-loop modifications, or B-box incrementation. Should these conditions arise, the trace routine will not be able to recognize an error interrupt. Further errors may result.
12. Error interrupts occurring in the user's interrupt routine or from I/O interrupt coding are not traced but proceed according to the logic of the monitor system.

#### Trace Program Logic

To provide complete information, an adequate trace program must contain a software trace to complement the 1107 hardware trace facility. The software component of this routine saves register R3 (normally used to hold memory lockout information) from destruction by the trace interrupt; prevents I/O

interrupts at critical phases, to assure no changes in R3 can be made during interrupt coding; obtains the address of all traced MOJP instructions (not provided by hardware); and detects all instructions executing skips.

The software trace component performs these duties in the following sequence:

1. Establishes address of next sequential instruction
2. Prevents all I/O interrupts
3. Saves contents of register R3
4. Obtains operation code of next sequential instruction, and performs special functions on an exceptional set of operations
5. Restores all thin film registers used by the trace routine
6. Establishes hardware trace mode
7. Executes remotely on next sequential instruction
8. If the instruction was not a jump, sets switch to show if a skip was executed
9. Saves R3 in event it was changed by a load or store
10. Jumps to routines to process all non-jump instructions

The exceptional set of operations occurs principally because of limitations placed upon executing remotely or by the I/O scheme used by the trace routine. Specifically, instructions SLJ and LMJ must not be executed remotely by the trace routine, for the return address would be incorrect. The instructions PAIJ and AAIJ must be sensed in order to inform later parts of the program to leave I/O in the desired state. Also, AAIJ must not be performed then but must be delayed until the trace interrupt occurs. Tests for nesting of instruction EX must be made to assure that previously mentioned instructions are not obscured.

The hardware component of the trace routine performs the following tasks:

1. Restores R3, which was destroyed by trace interrupt

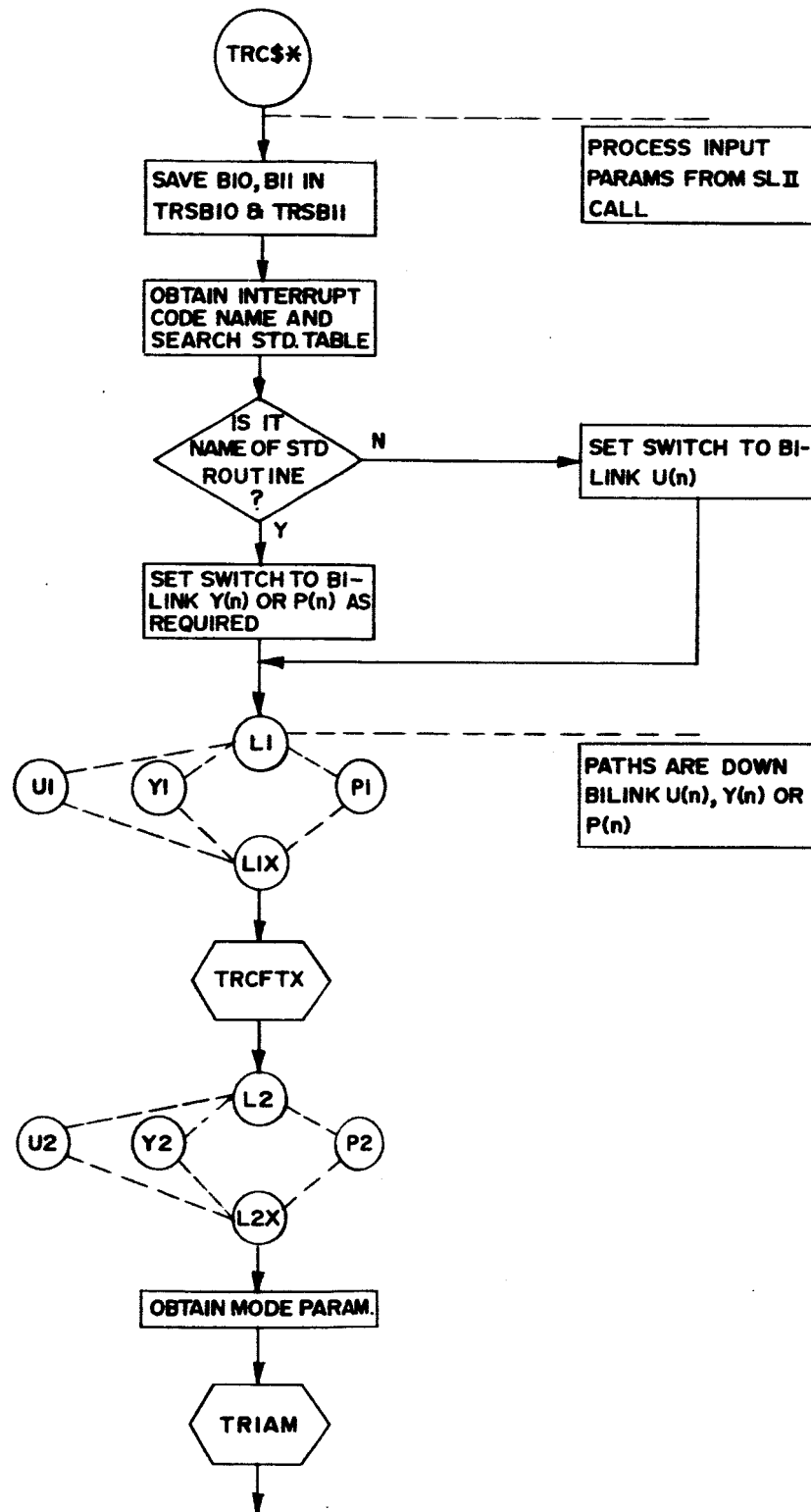
2. Restores I/O interrupt state to that expected by traced program
3. Obtains the destination address of the traced jump, and performs special functions on an exceptional set
4. Determines if the jump was intended as an entry into trace routine itself; if so, allows it
5. Determines if the jump origin or destination address is in user's core; if so, calls interrupt coding
6. Transfers control back to the software trace component

Among the exceptional destination addresses are MREA\$ and MSEA\$. If a jump to MSEA\$ or MREA\$ is made, and if a request is made to reset MIALL\$ (all error actions) or to change MITRC\$ alone (the trace location), all thin film is restored to that expected by the external program, and tracing is terminated.

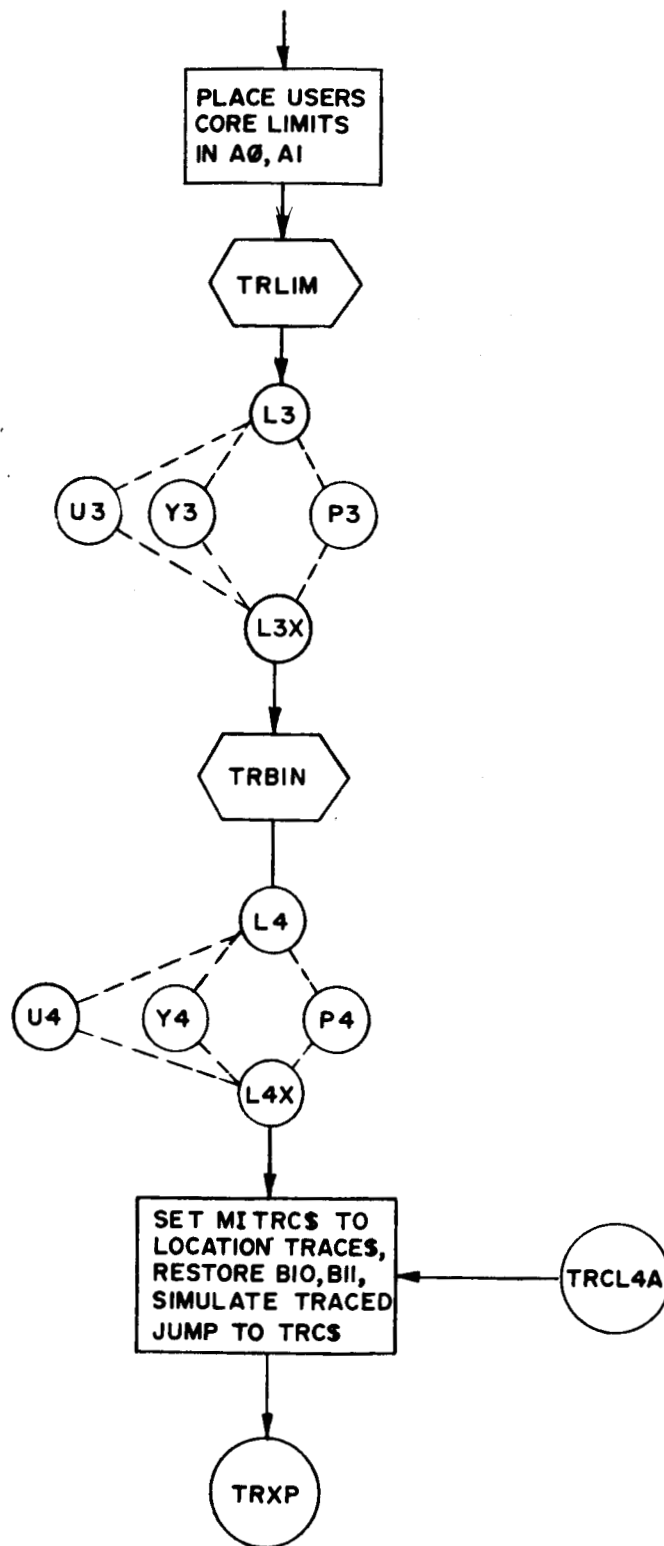
The other exceptional addresses are concerned with error interrupt destinations. If a match of the intended destination of an instruction to the BHIU- fields of the instruction in an error interrupt location is found, it is assumed an error interrupt just occurred. Special testing and correcting procedures are then followed to ensure that the true error address is reported to the error routine, rather than the address of the execute remote in the trace program.



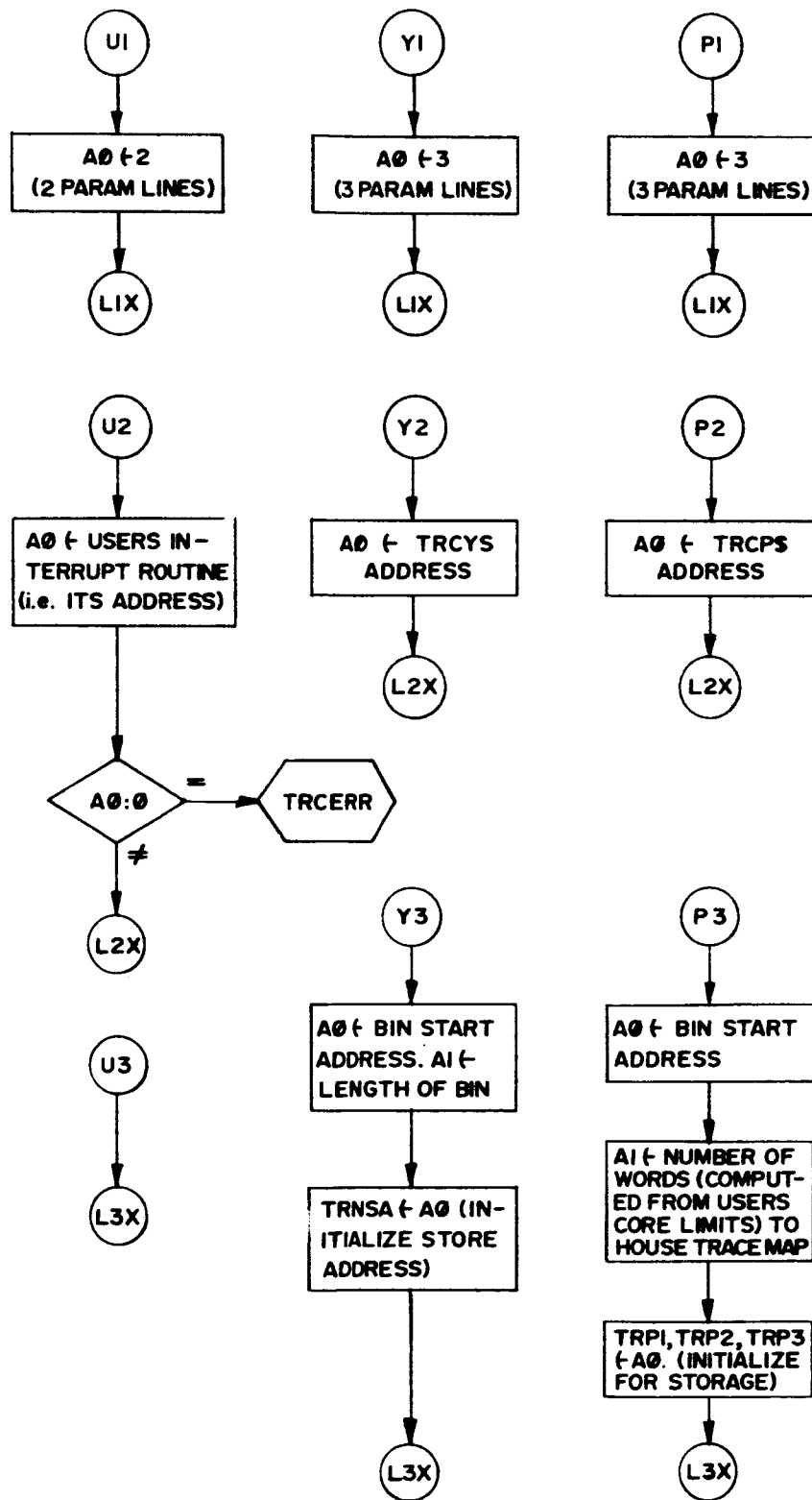
## APPENDIX: TRACE ROUTINE FLOW DIAGRAMS



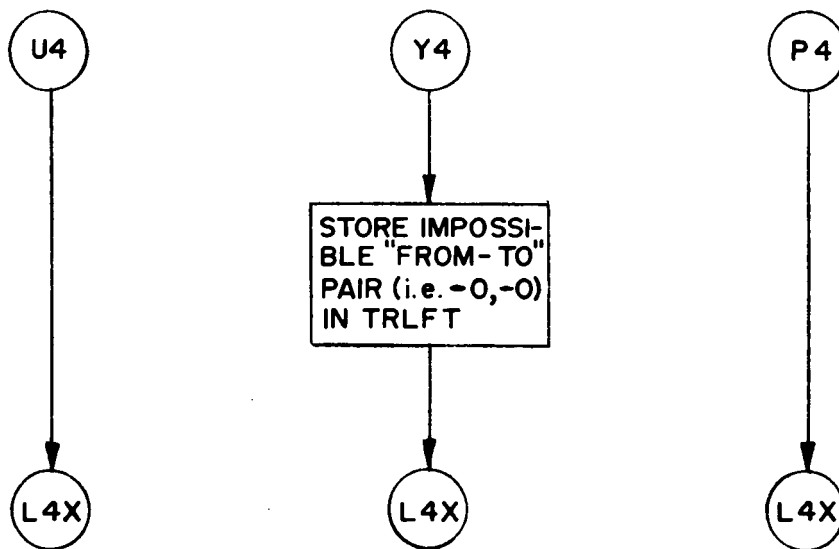
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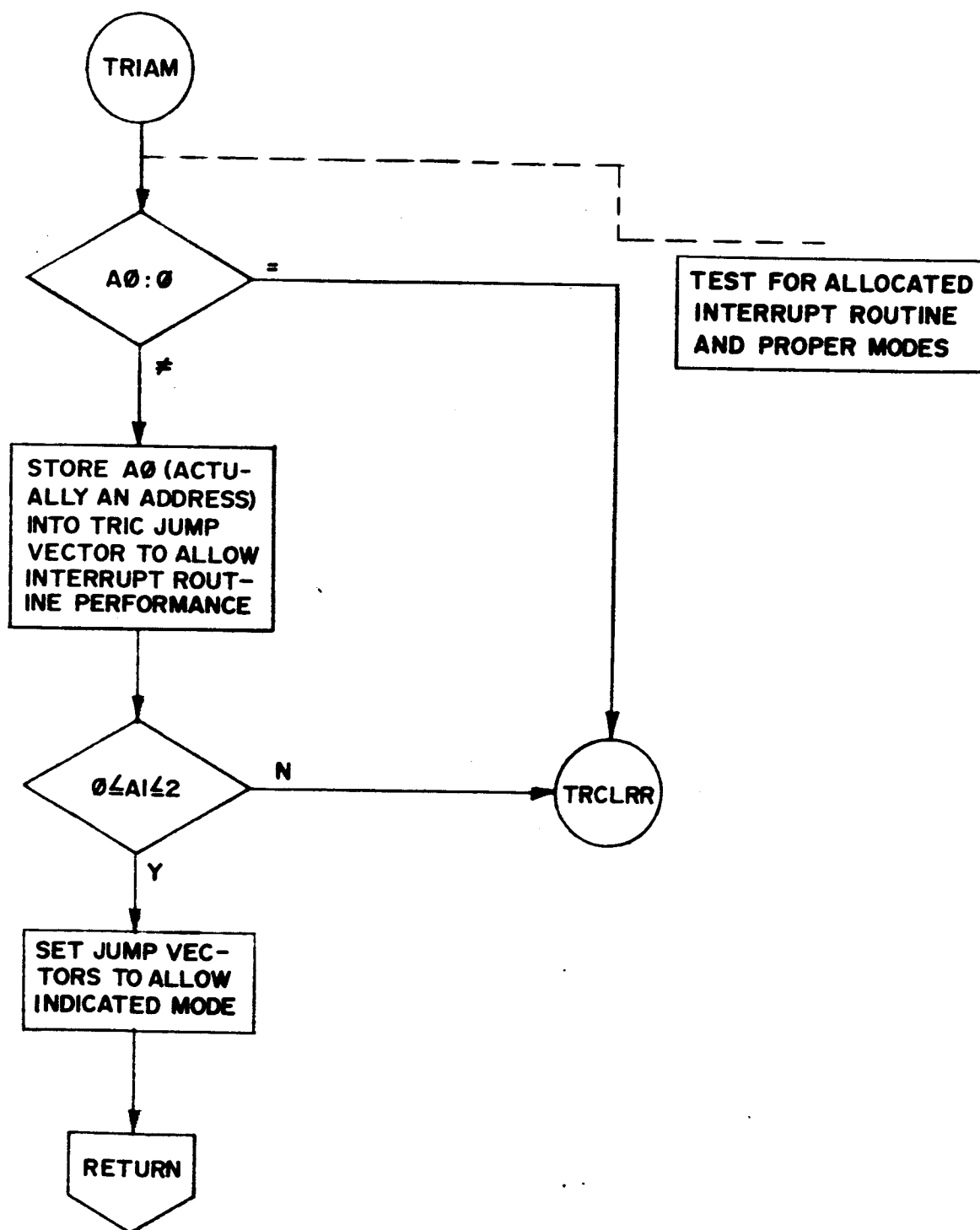
Trace 2



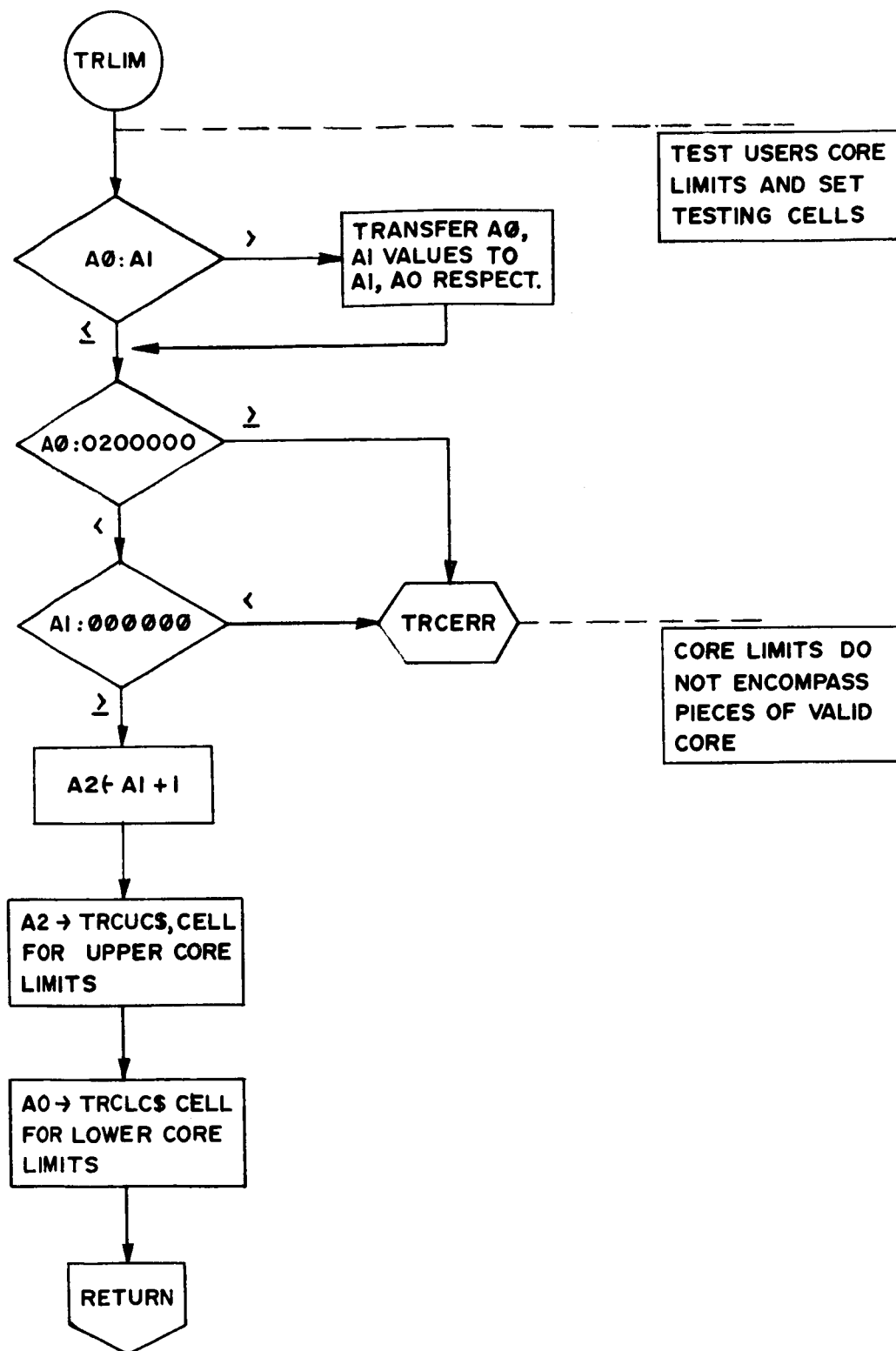
Trace 3



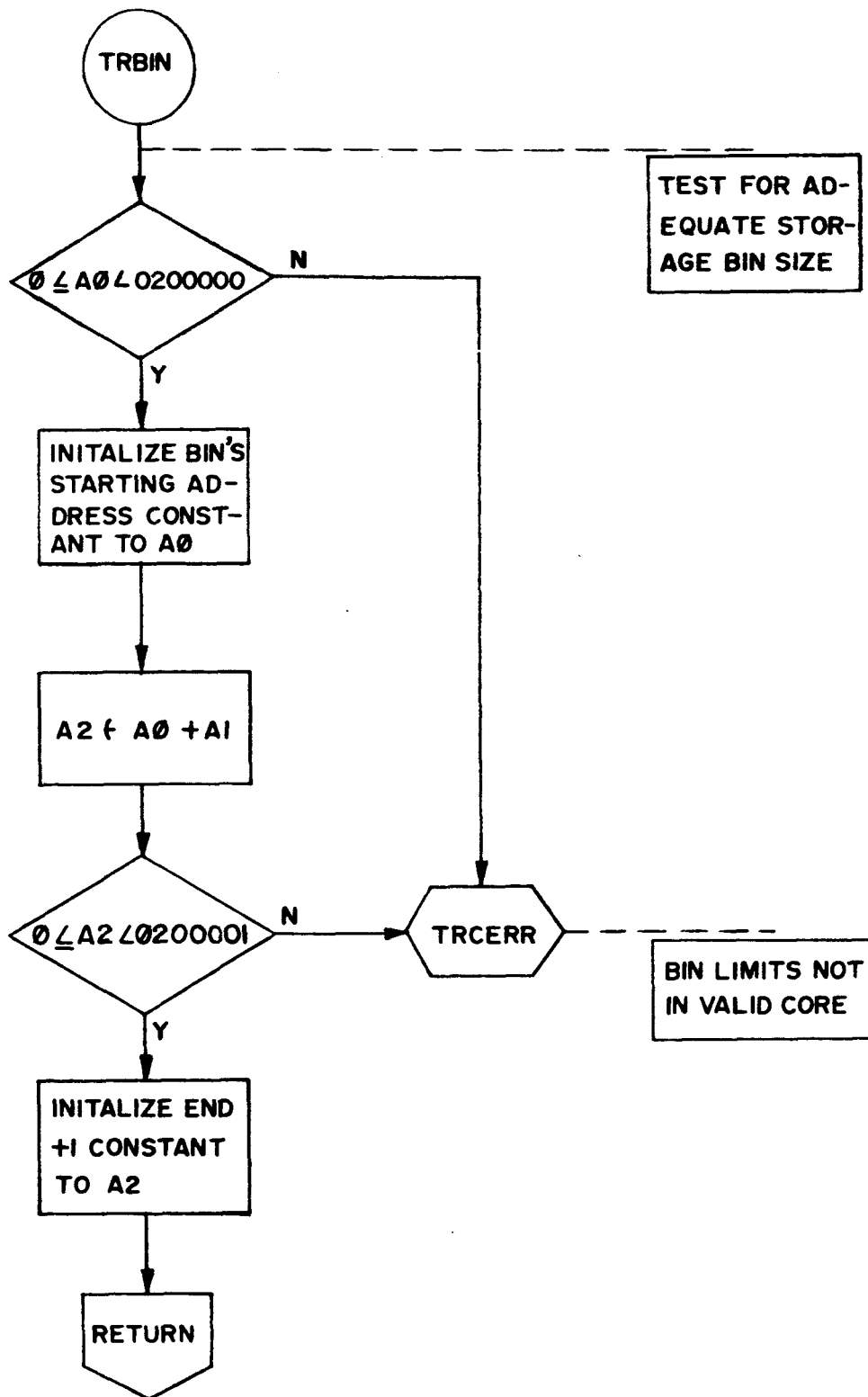
Trace 4



Trace 5

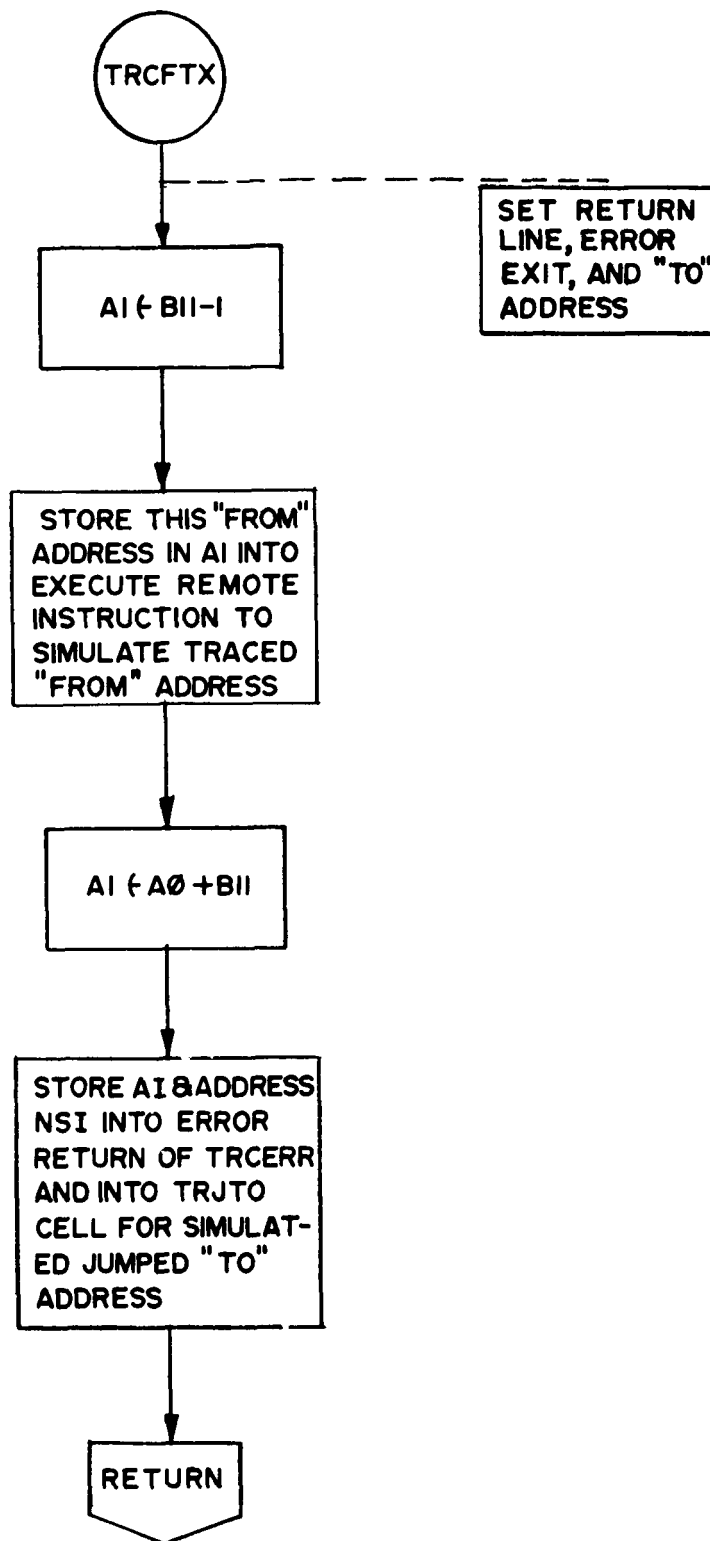


Trace 6

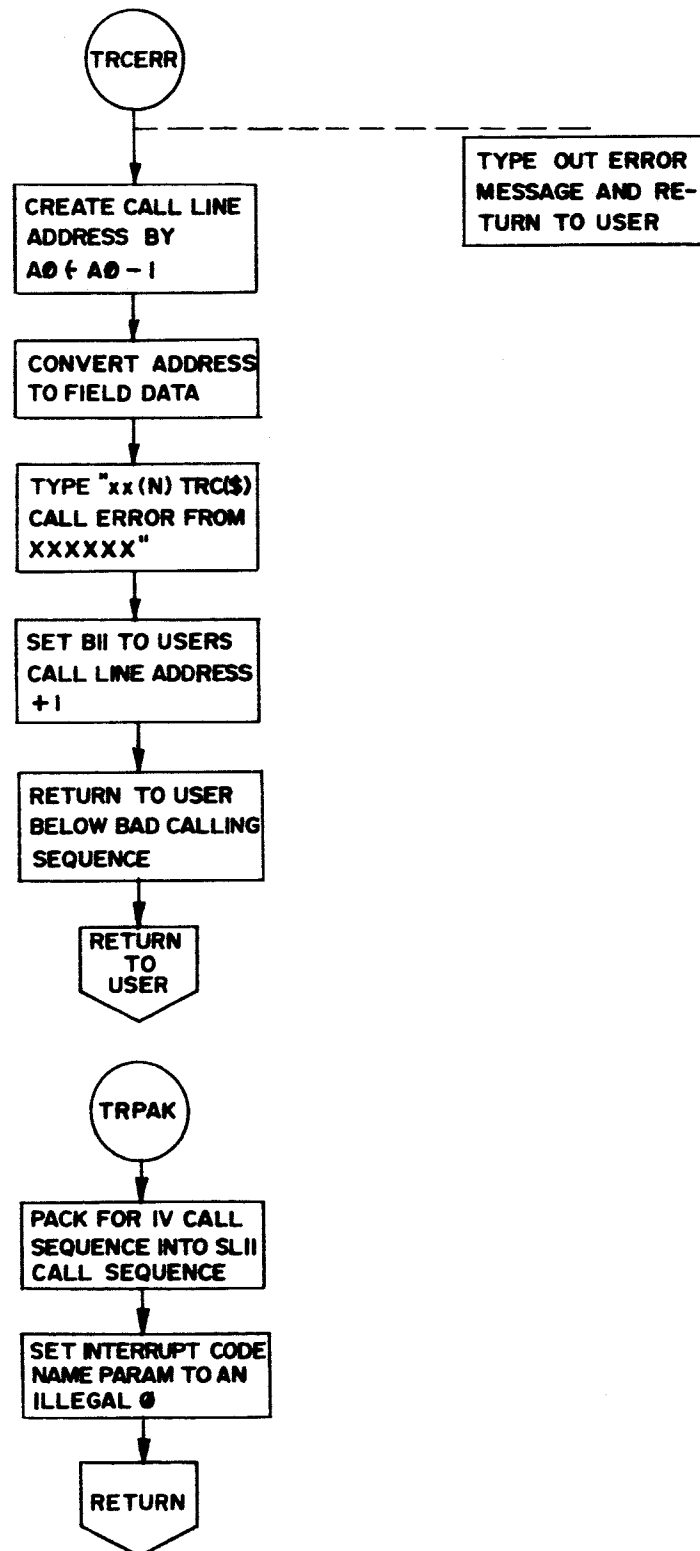


Trace 7

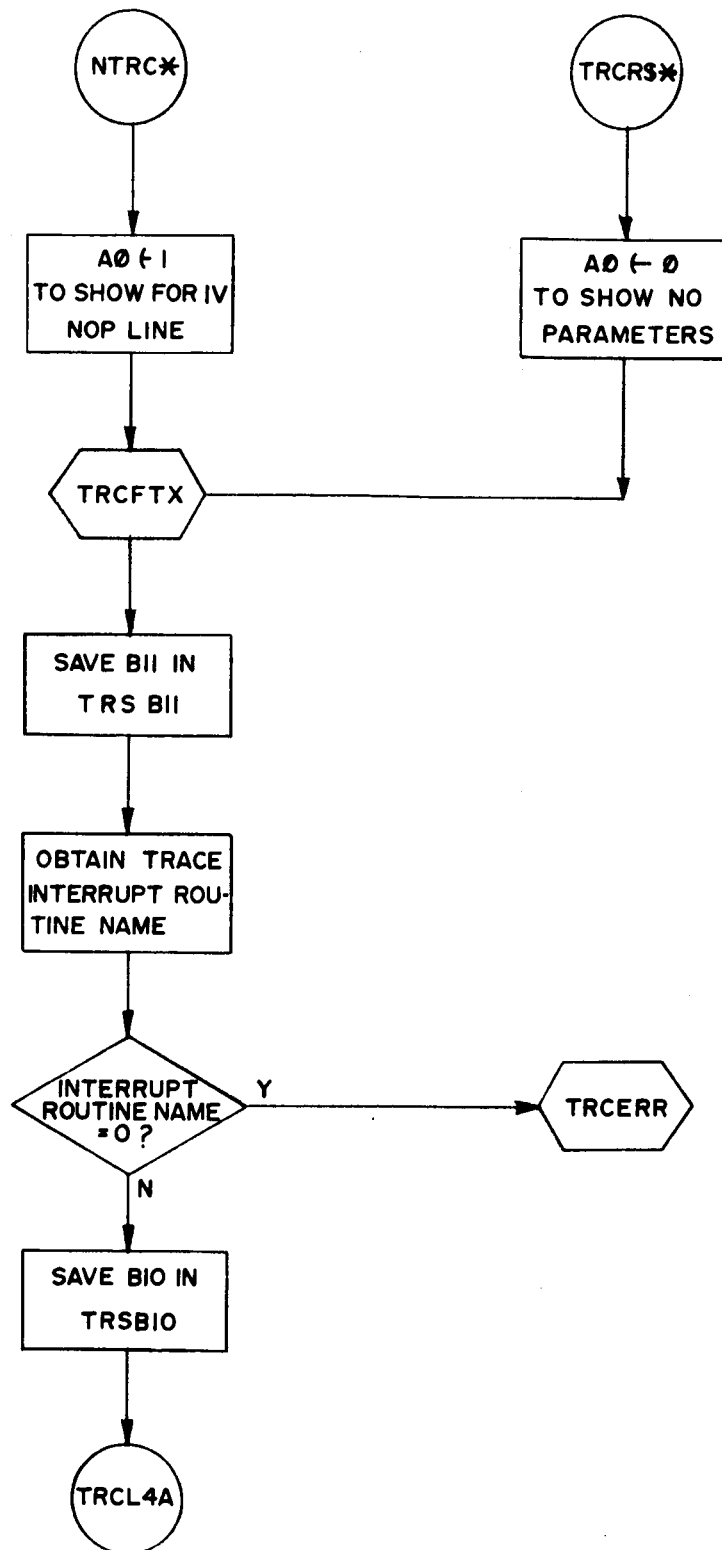




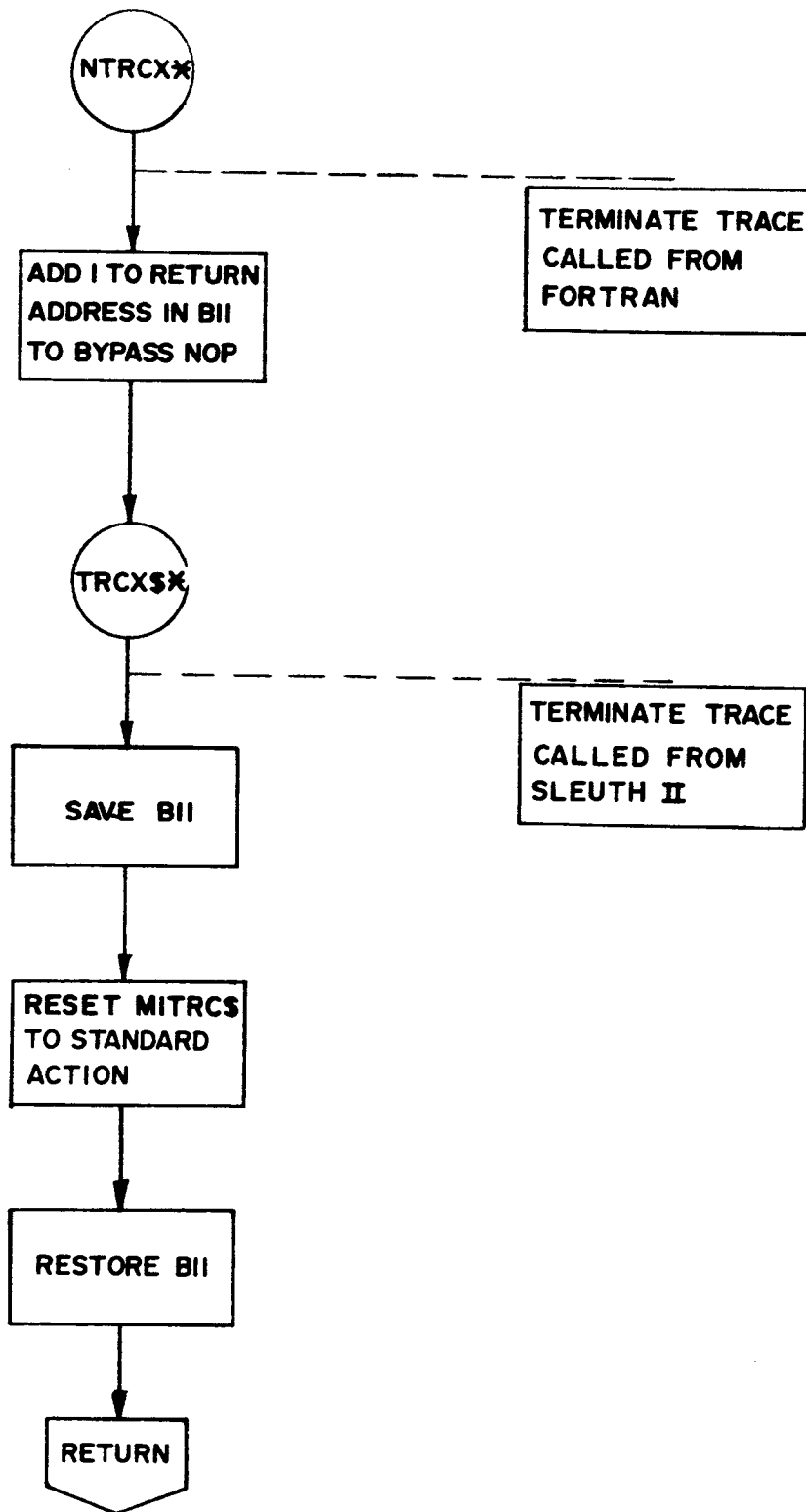
Trace 8



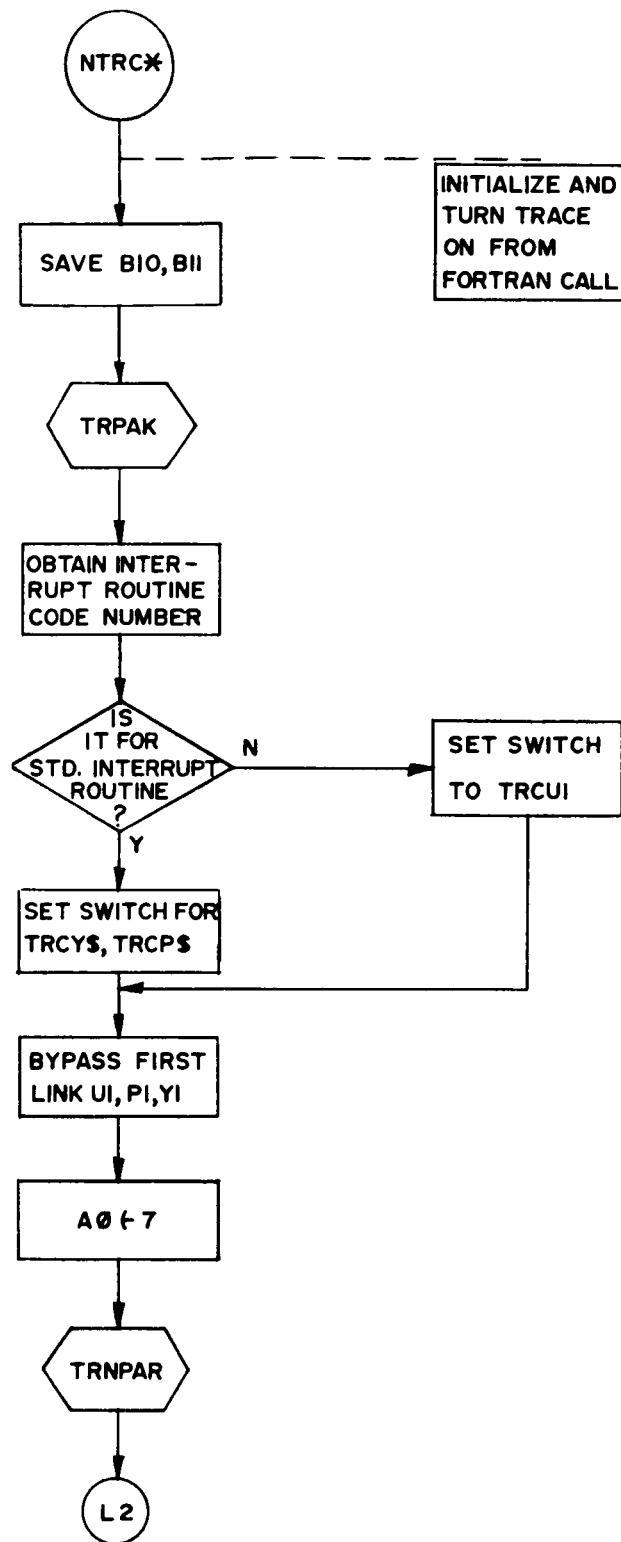
Trace 9



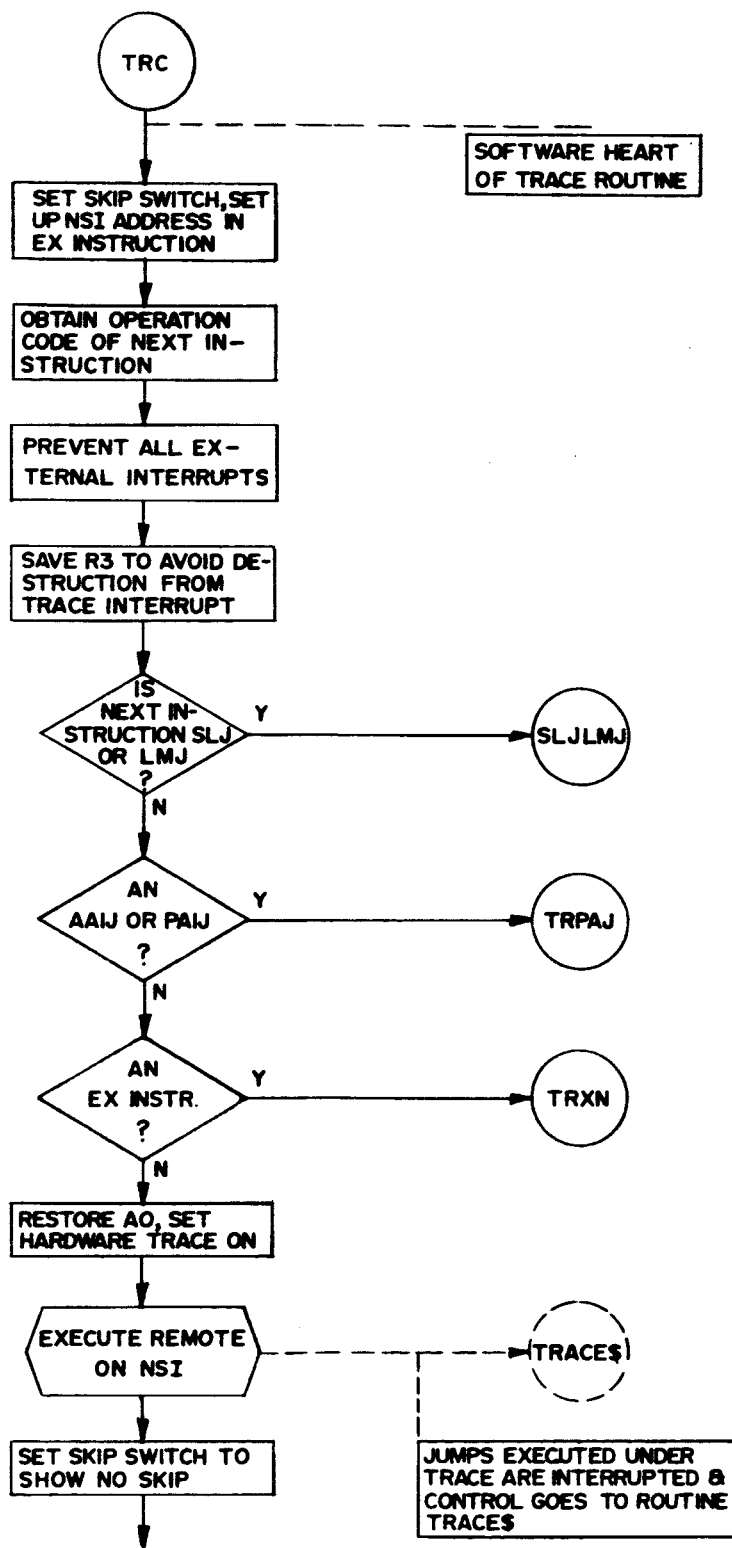
Trace 10



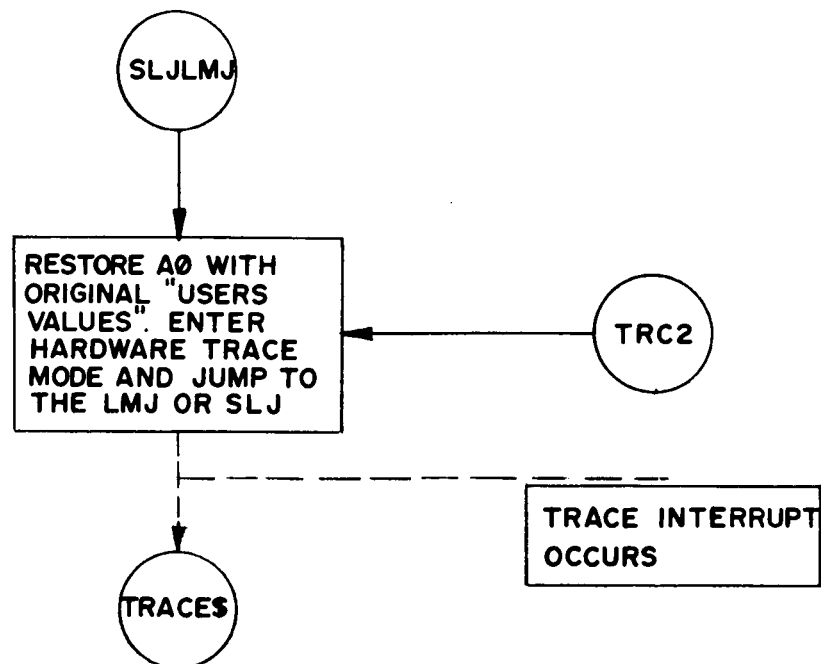
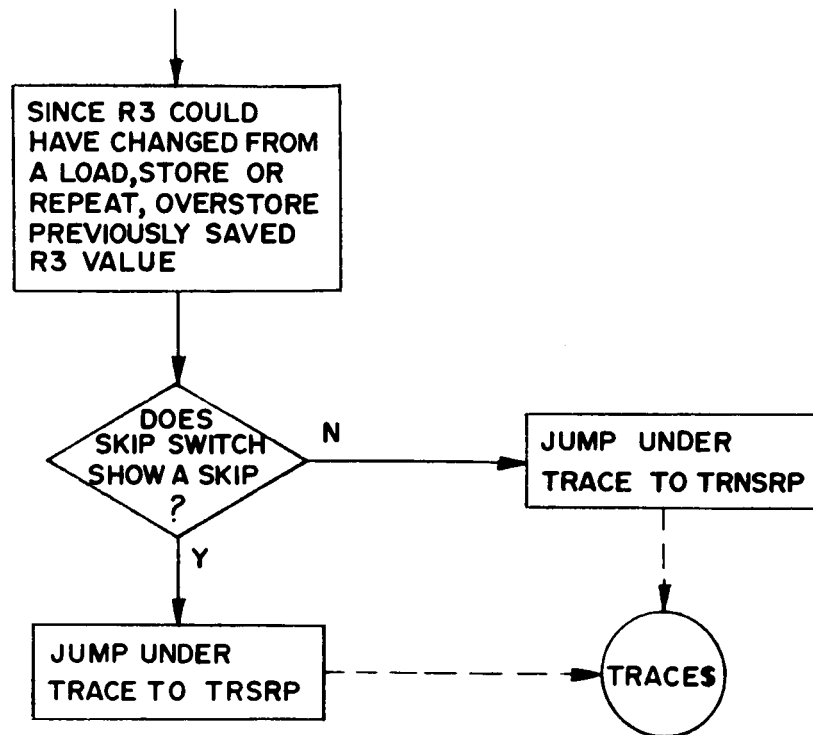
Trace 11



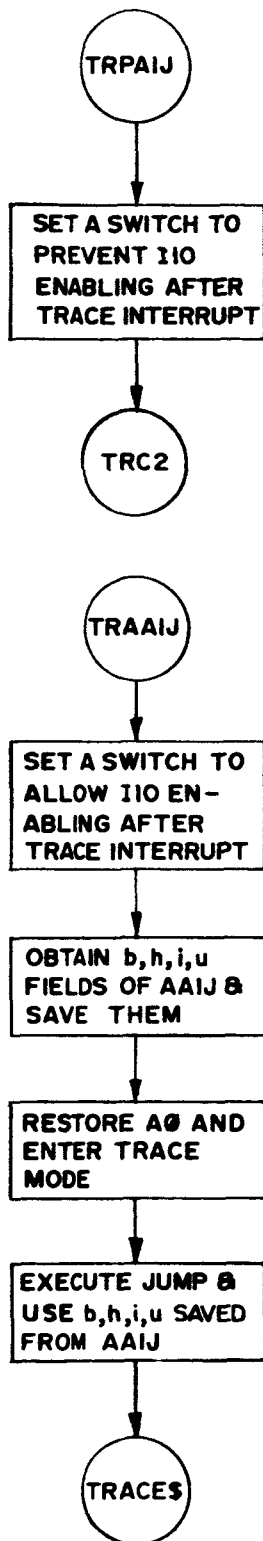
Trace 12



Trace 13

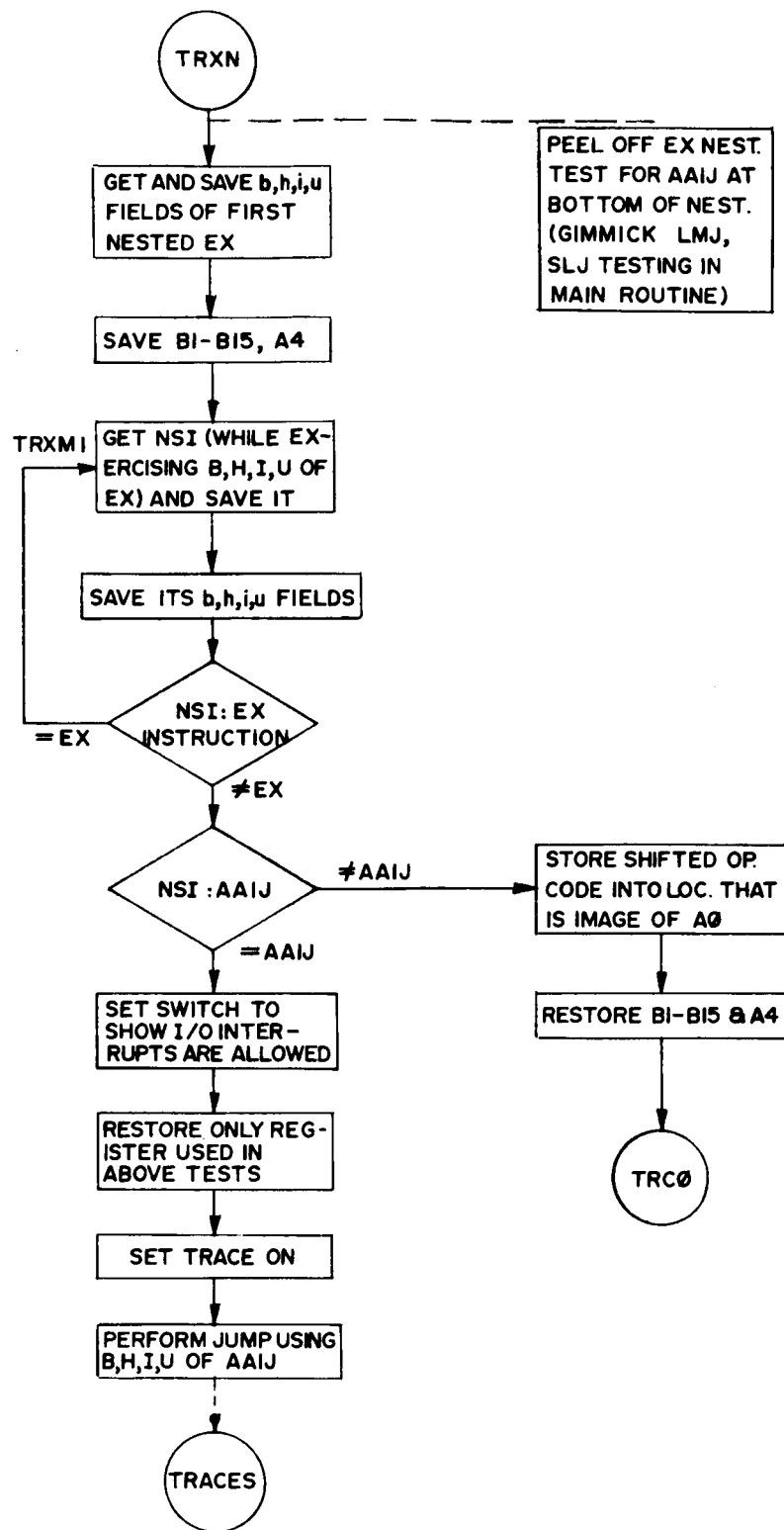


Trace 14

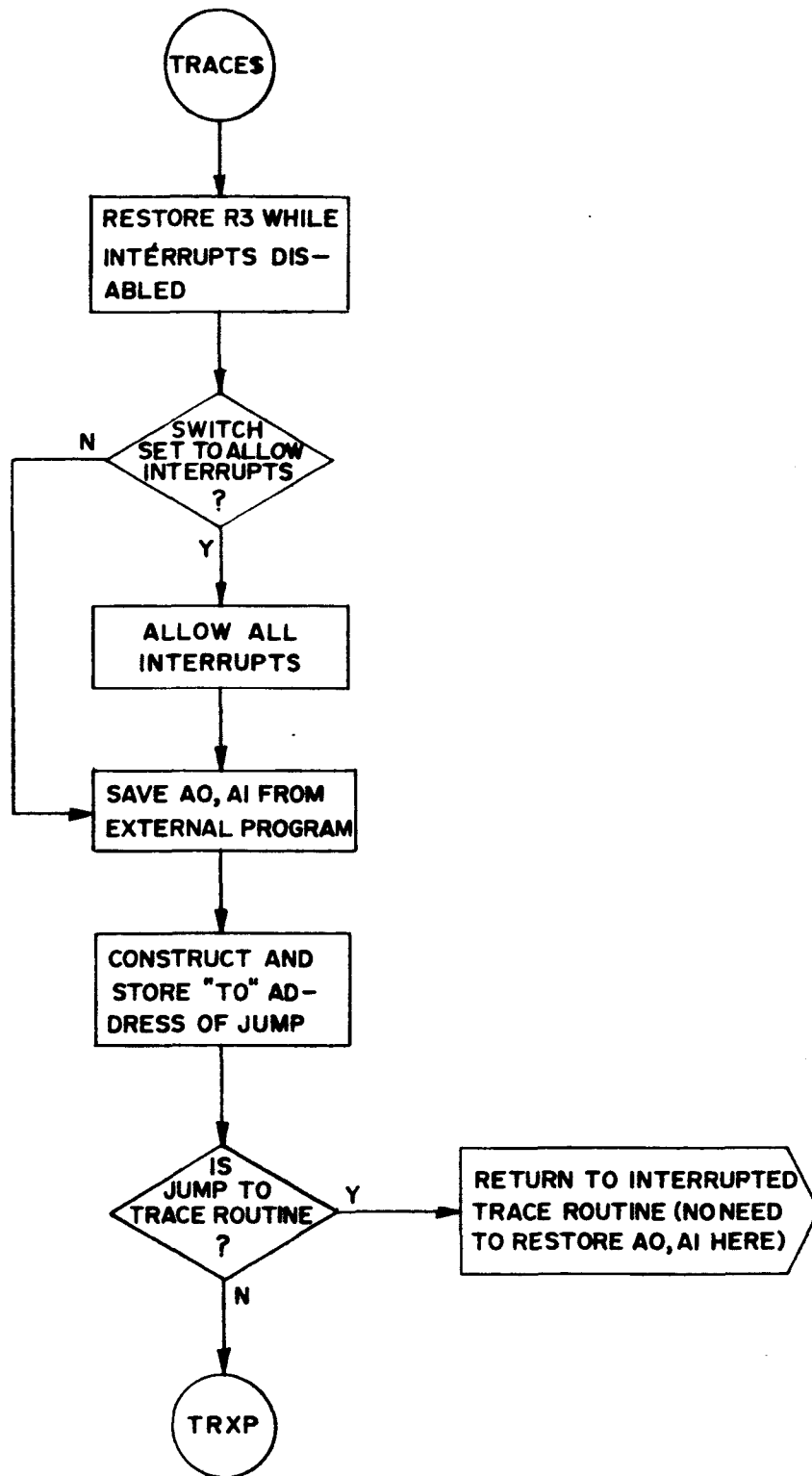


Trace 15

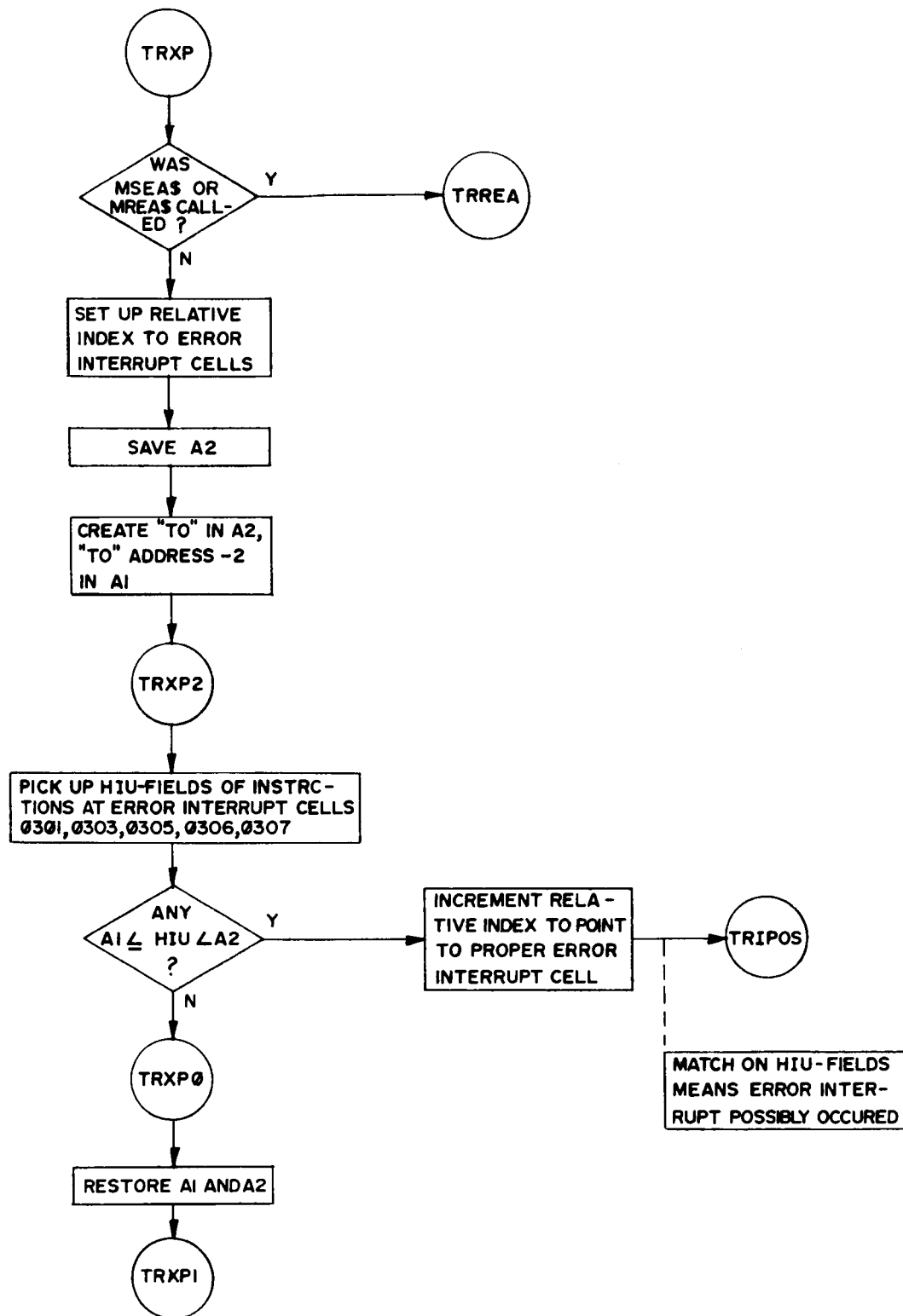




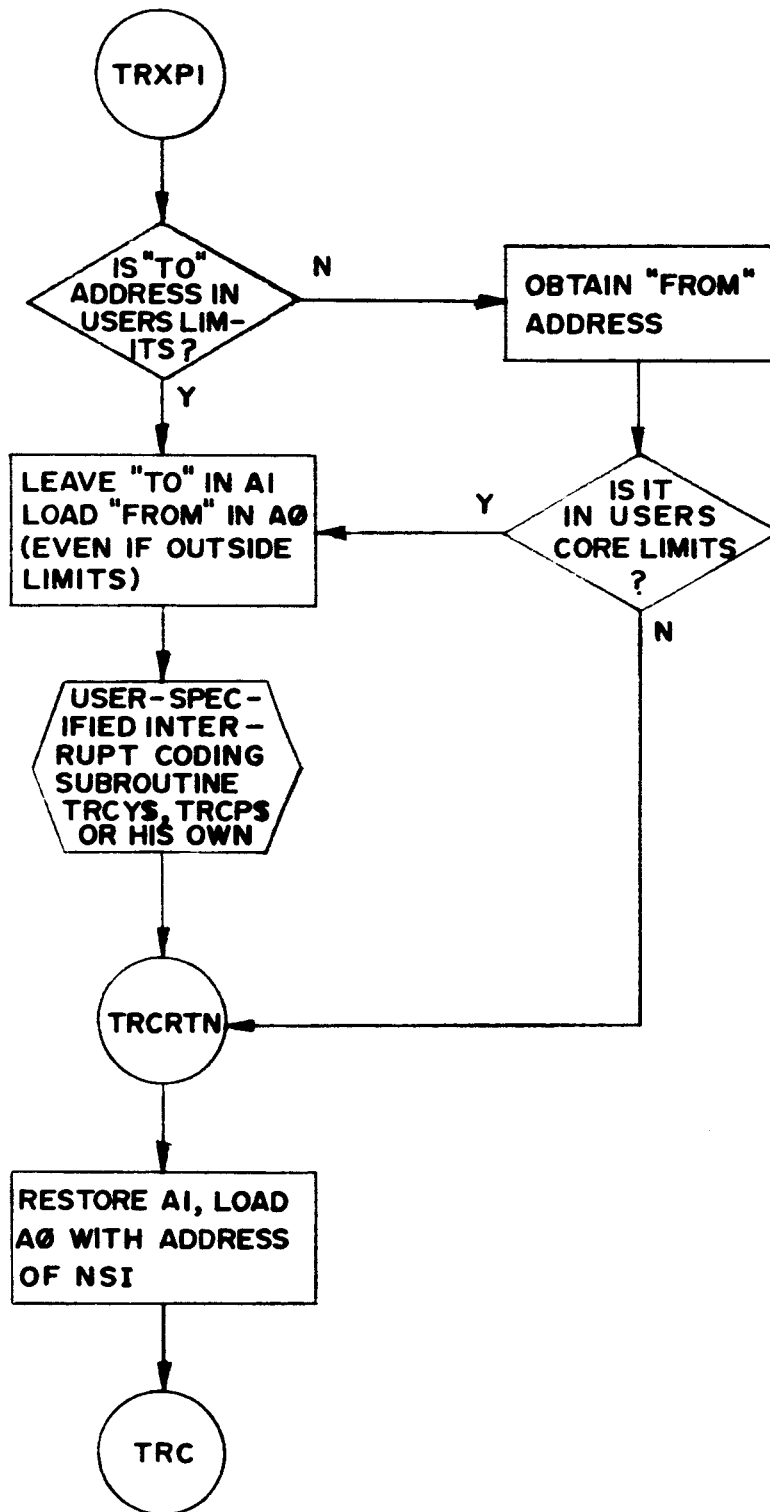
Trace 16



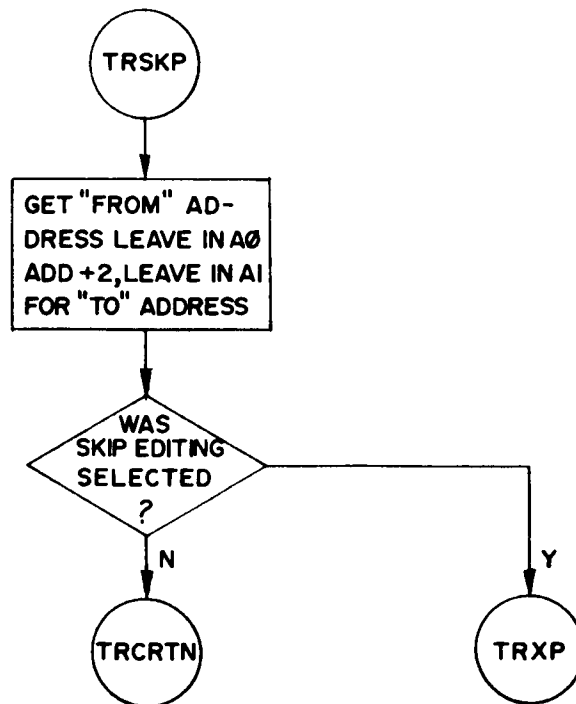
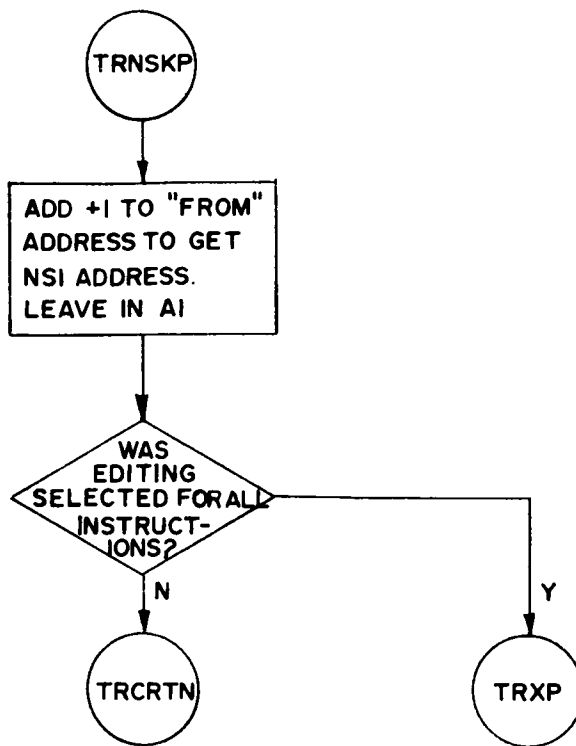
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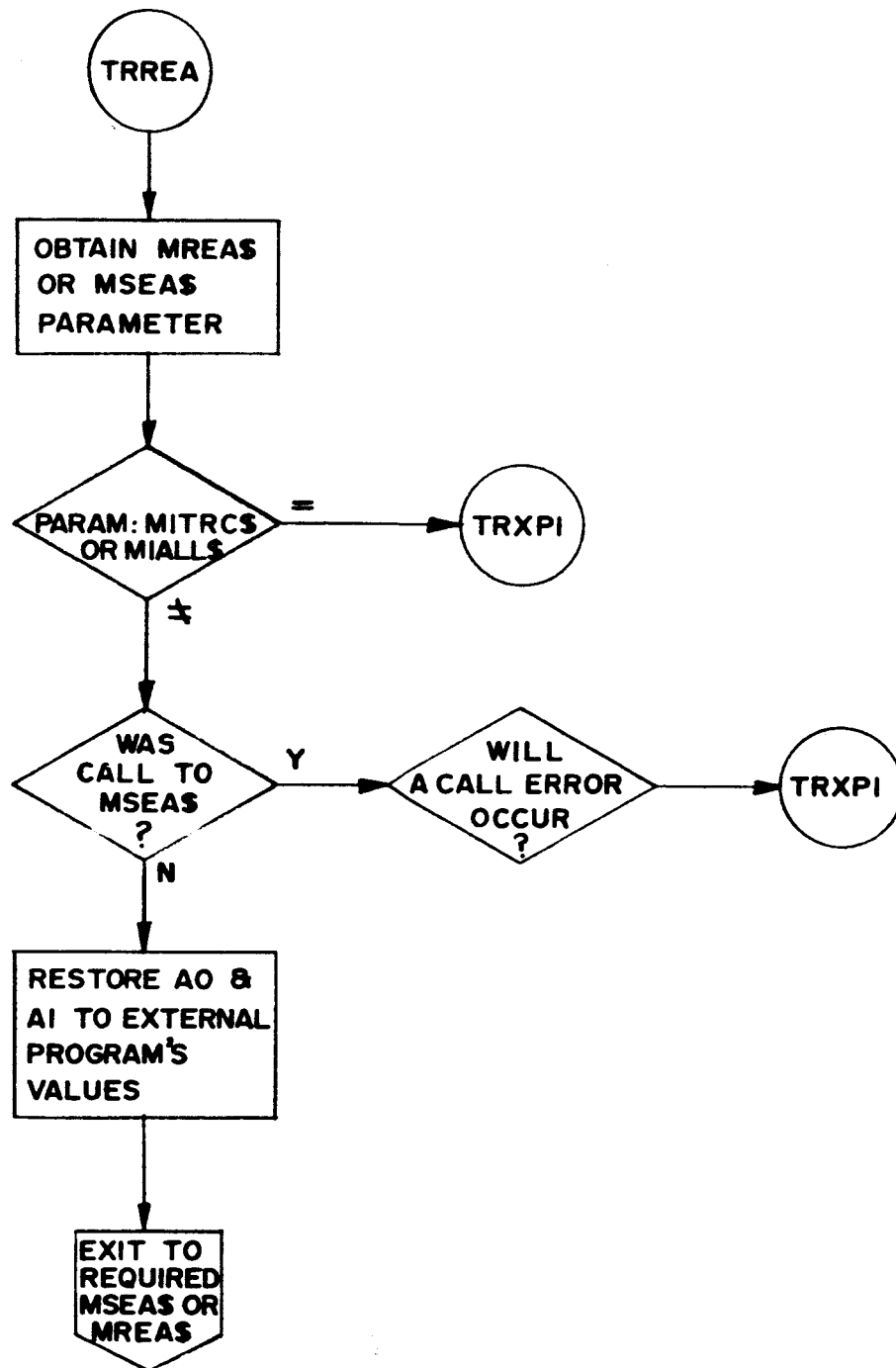
Trace 18



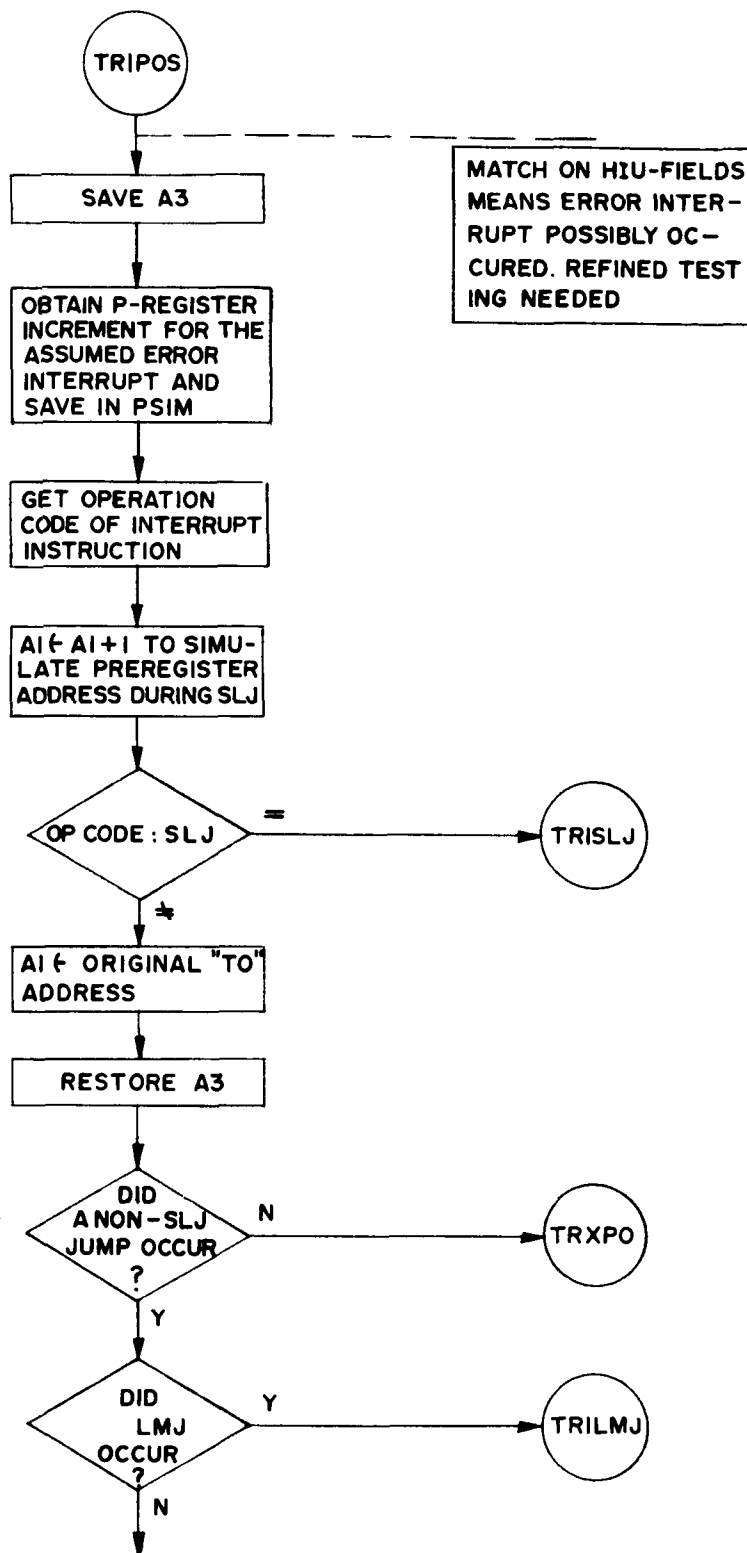
Trace 19



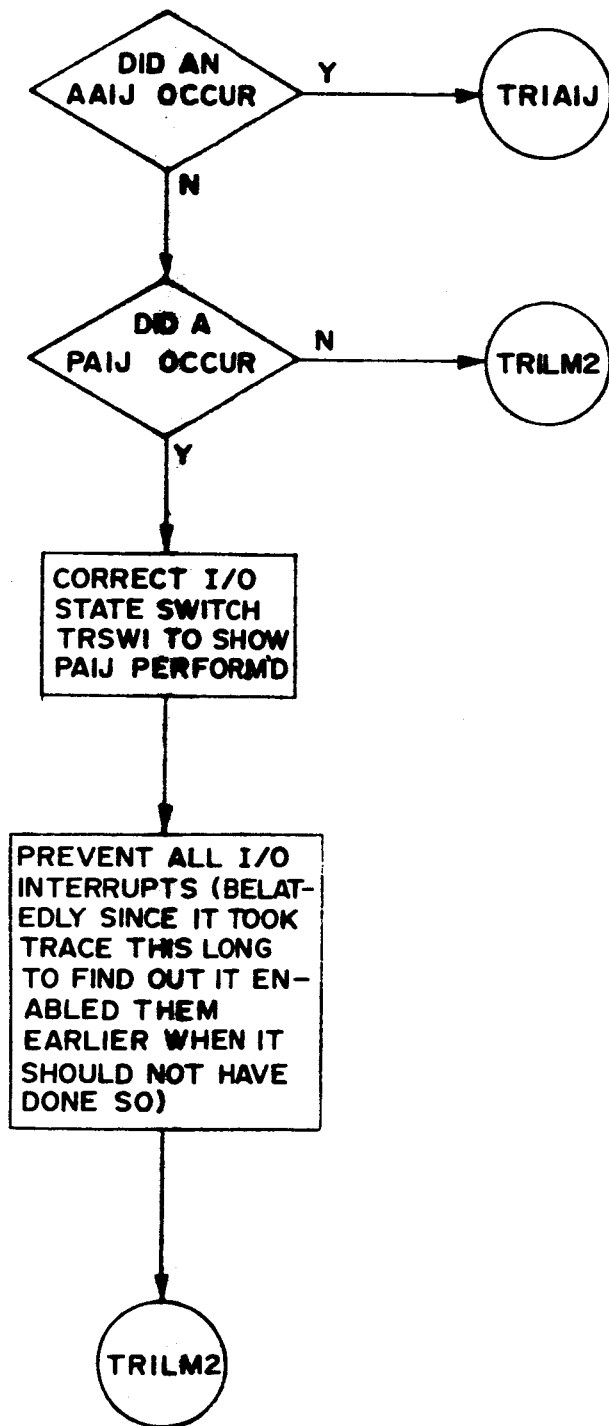
Trace 20



Trace 21

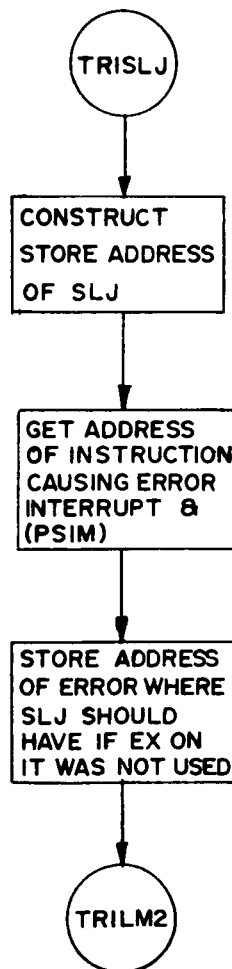
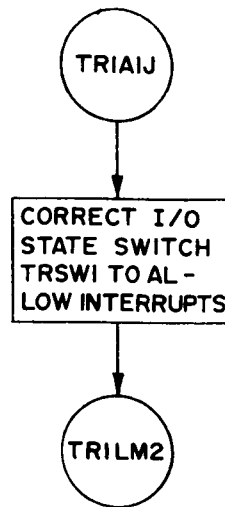


Trace 22

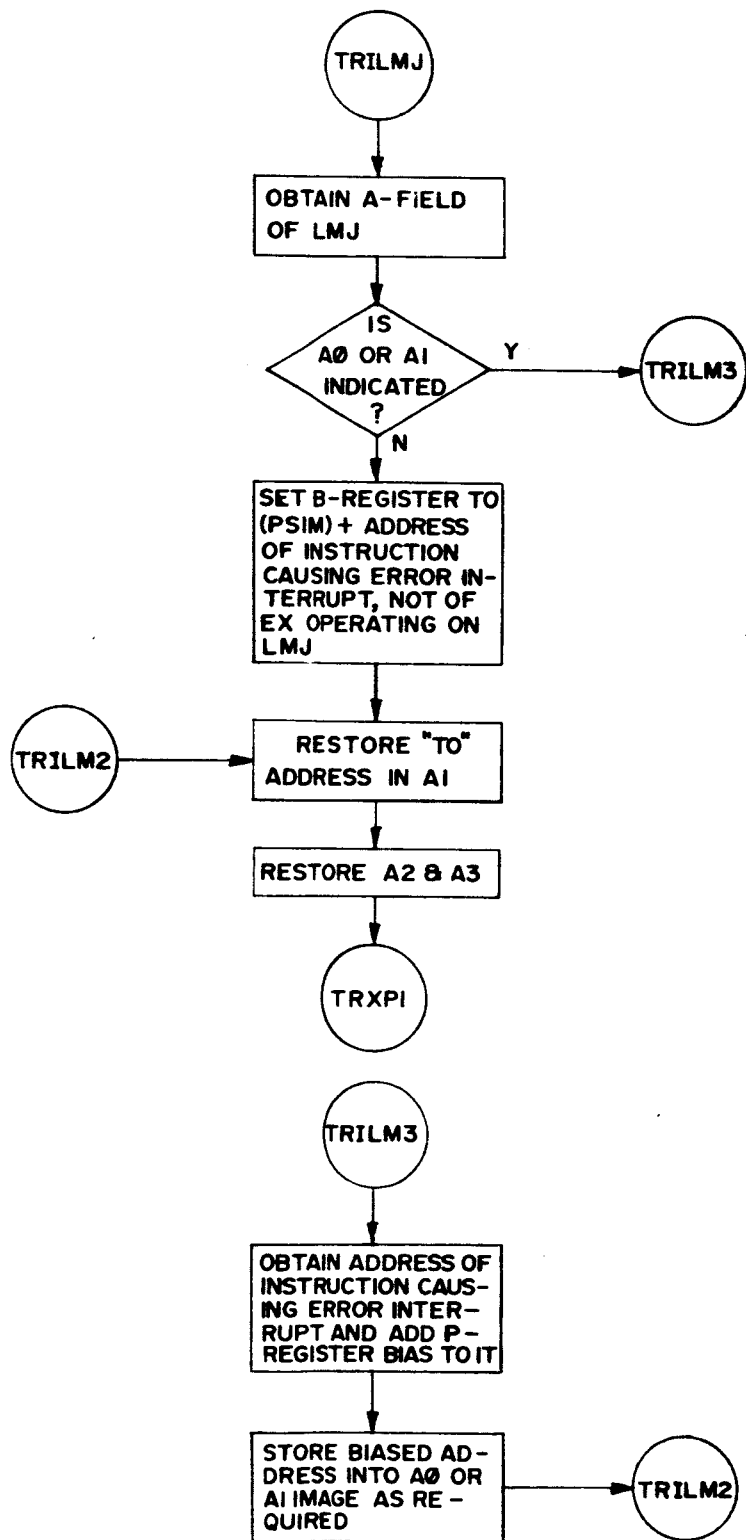


Trace 23

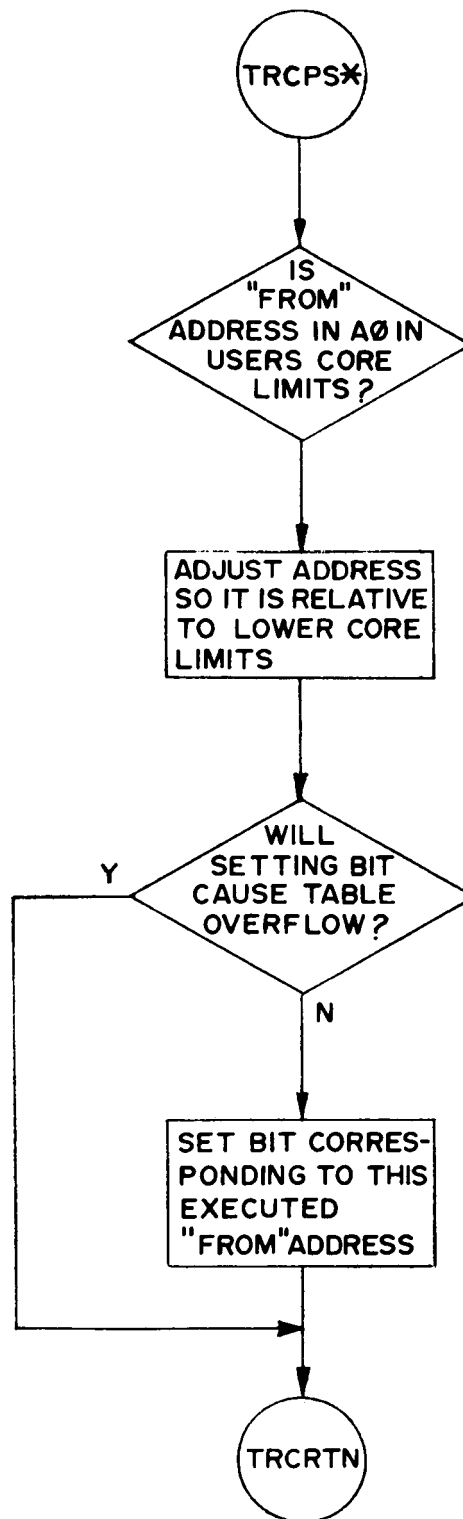




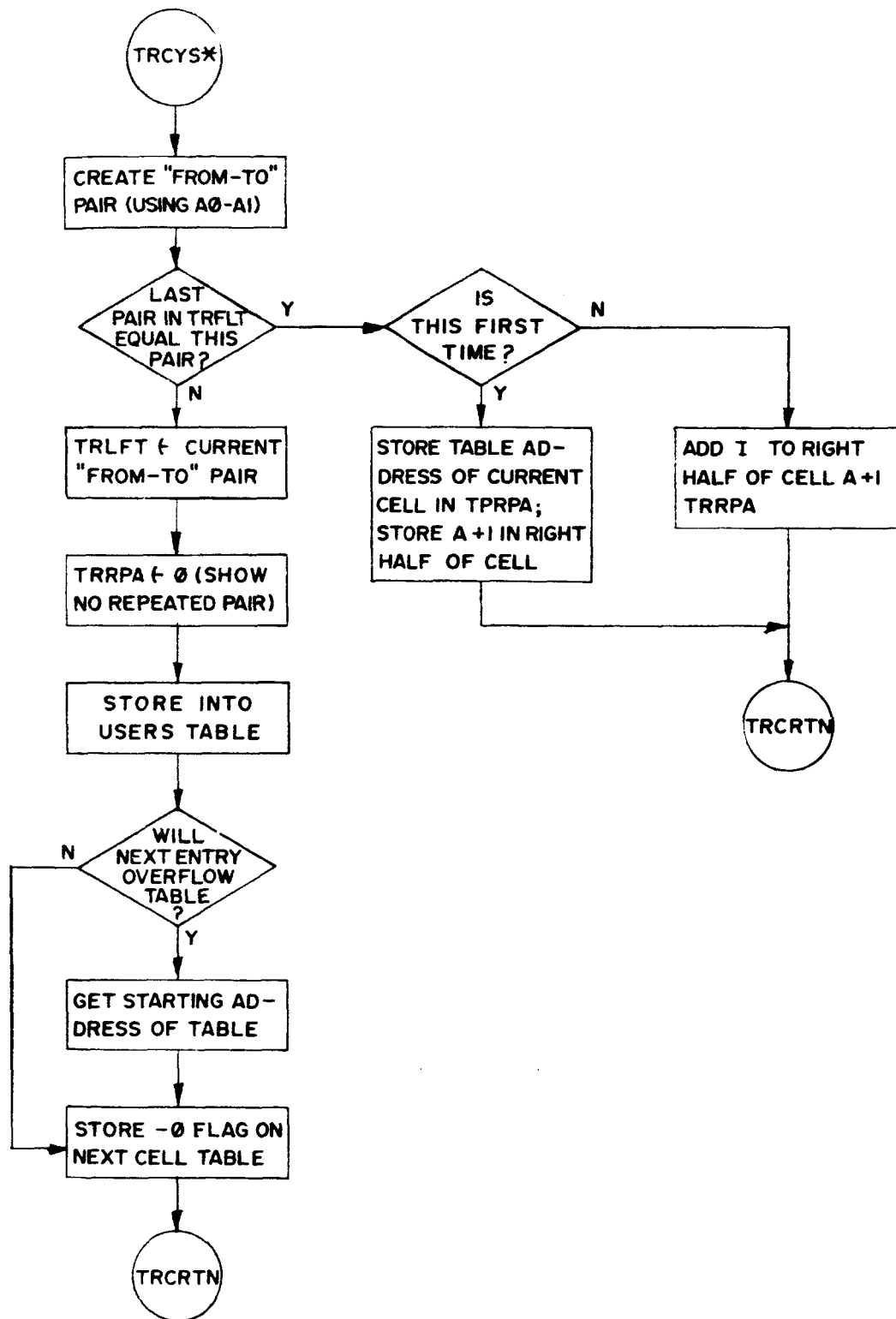
Trace 24



Trace 25



Trace 26



Trace 27

LIA\* ASK\*\* TRACE  
 ASSEMBLED BY UNIVAC 1107 SLEUTH 11 DATED- JANUARY 3-1964  
 THIS ASSEMBLY WAS DONE ON 01 APR 65 AT 08:06:14

000001	A0	0000000014	EQ	14
000002	A1	00000000015	EQ	15
000003	A2	00000000016	EQ	14
000004	A3	00000000017	EQ	15
000005	A4	00000000020	EQ	16
000006	B10	00000000012	EQ	10
000007	B11	00000000013	EQ	11
000008	MLC	00000000010	EQ	67
000009	R1	00000000010	EQ	67
000010	R3	00000000010	EQ	67
000011	FILL	77777777777	EQ	-U
000012	S(1)		INFO	5
000013	TPFA		B11+ERRS	1
000014			LMU	B11+ERRS
000015			LMU	B11+ERRS

01 000010 74 13 13 00 0 0001015  
 000001 74 13 13 00 0 0001015

/ SET UP PARAMETERS SURROUTINES

000019	TP1AM	74 04 00 00 0 000002	J	5
000020		* 20-35 +CC 1	JZ	A0+TRCERR
000021		74 00 00 00 0 000056		
000022		* 20-35 +CC 1	S+1	A0+TRIC
000023		74 01 14 00 0 000411	TL+14	A1+4
000024		* 20-35 +CC 1	TP	A1
000025		74 00 00 00 0 000015	J	TRCERR
000026		* 20-35 +CC 1	L+14	A2+TRCERR
000027		74 16 16 00 0 000412	L+14	A3+TRAP
000028		* 20-35 +CC 1	S+1	A2+TRSKP1
000029		74 01 16 00 0 000430	S+1	A2+TRASK1
000030		* 20-35 +CC 1	TZ	A1
000031		74 01 17 00 0 000430	S+1	A3+TRSKP1
000032		* 20-35 +CC 1	TL+14	A1+2
000033		74 01 16 00 0 000424	S+1	A3+TRASK1
000034		* 20-35 +CC 1	J	TR1AM
000035		74 04 00 00 0 000002	J	5
000036		* 20-35 +CC 1	TL	A1+40
000037		74 00 01 00 0 000014	DS	A0+36
000038		* 20-35 +CC 1	TL	A0+(02000000)
000039		74 01 16 00 0 000000	TL+14	A1+0
000040		* 20-35 +CC 1	J	TRCERR

• INDEPENDENT TO AVOID OVERLAY  
 • FIRST GENERATED LINE (ALSO GUARD LINE)  
 • GUARD LINE FOR ILLEGAL ENTRANCE

• A0=INTERRUPT ADDRESS SWITCH A1=MODE  
 • ADDRESS SWITCH ILLEGAL  
 • SWITCH IS ACTUALLY INTERRUPT CODE TAG

• MODE ERROR

• MODE 0 = JUMPS ONLY

• MODE 1 = JUMPS AND SKIPS

• MODE 2 = ALL INSTRUCTIONS

• A0=LOW CORE LIMITS, A1=UPPER LIMITS

• CORRECT LIMITS REVERSAL  
 • TEST WITHIN PHYSICAL CORE

[illegible]

ADDRESS	DATA	TPPAK	J	COMMENT
000074	74 04 00 00 0 000066			• FOR IV PAK INTO SLII PARAMS
000075	* 40-35 +CC 1			• ILLEGAL INTERRUPT CODE NAME FOR
000076	05 02 00 00 0 000064		SZ+2	• LATER POSSIBLE CALL ERROR
000077	* 40-35 +CC 0			• MODE
000078	000070 27 00 14 13 1 000001		L	• LOWER CORE LIMITS
000079	000071 06 01 14 00 0 000064		S+1	• UPPER CORE LIMITS
000080	* 40-35 +CC 0			• BIN ADDRESS
000081	000072 27 00 14 13 0 000002		L	• BIN LENGTH
000082	000073 06 02 14 00 0 000065		S+2	
000083	* 40-35 +CC 0			
000084	000074 27 00 14 13 0 000003		L	
000085	000075 06 01 14 00 0 000065		S+1	
000086	* 40-35 +CC 0			
000087	000076 27 00 14 13 0 000004		L	
000088	000077 06 02 14 00 0 000066		S+2	
000089	* 40-35 +CC 0			
000090	000100 27 00 14 13 1 000005		L	
000091	000101 06 01 14 00 0 000066		S+1	
000092	* 40-35 +CC 0			
000093	000102 74 04 00 00 0 000066		J	
000094	* 40-35 +CC 1			
000095	000103 06 00 13 00 0 000043		S	• ENTRY POINTS AND INTERRUPT CODING INITIALIZATION
000096	* 40-35 +CC 0			
000097	000104 06 00 12 00 0 000042		S	
000098	* 40-35 +CC 0			
000099	000105 23 16 01 00 0 000003		L+04	• SEARCH TRACE VECTOR TABLE
000100	000106 27 00 14 00 0 000100		L	
000101	* 40-35 +CC 0			
000102	000107 27 02 15 13 0 000000		L+2	• INTERRUPT ROUTINE SWITCH
000103	000110 62 02 01 14 2 000022		SE+2	• TEST FOR STD. INTERRUPT CODE NAME
000104	* 40-35 +CC 0			
000105	000111 05 00 00 00 0 000014		SZ	• NOT STANDARD
000106	000112 27 01 14 14 0 000021		L+1	
000107	* 40-35 +CC 0			
000108	000113 74 13 12 14 0 000000		PRIME LINK	• GET NO. PAKAM LINES
000109	000114 72 01 00 00 0 000046		TRCL1	
000110	* 40-35 +CC 1		SLJ	
000111	000115 74 13 12 12 0 000000		TRCL2	• GET INTERRUPT LOCATION
000112	000116 27 01 15 13 0 000000		L+1	• GET MODE
000113	000117 72 01 00 00 0 000002		SLJ	
000114	* 40-35 +CC 1			
000115	000120 27 02 14 13 0 000001		L+2	• LOWER CORE ADDRESS
000116	000121 27 01 15 13 0 000001		L+1	• UPPER CORE ADDRESS
000117	000122 72 01 00 00 0 000021		SLJ	• CHECK THEM AND SET UP
000118	* 40-35 +CC 1			
000119	000123 74 13 12 12 0 000000		TRCL3	• GET BIN ADDRESS AND LENGTH
000120	000124 72 01 00 00 0 000033		SLJ	• CHECK THEM AND SET UP
000121	* 40-35 +CC 1			
000122	000125 74 13 12 12 0 000000		TRCL4	• SET MITRCS LOCATION
000123	000126 72 01 00 00 0 000033		TRCL4A	• TRACE RE-ENTRY POINT AFTER SET UP
000124	* 40-35 +CC 1			
000125	000127 74 13 12 12 0 000000			

ADDRESS	DATA	PC	PSW	STATUS	INSTR	COMMENT
000113	000126 74 13 13 00 0 000007					
	000127 000000 000003					
	000130 7204000000356					
	000131 27 00 13 00 0 000043					
000114	000132 06 02 13 00 0 000074					
000115	000133 27 00 12 00 0 000042					
000116	000134 27 01 15 00 0 000034					
000117	000135 74 04 00 00 0 000373					
000118	000136 27 16 14 00 0 000002					
000119	000137 74 13 12 12 0 000000					
000120	000140 27 02 14 13 0 000000					
000121	000141 74 00 00 00 0 000036					
000122	000142 74 13 12 12 0 000000					
000123	000143 74 13 12 12 0 000001					
000124	000144 74 13 12 12 0 000000					
000125	000145 27 16 14 00 0 000003					
000126	000146 74 13 12 12 0 000000					
000127	000147 27 16 14 00 0 000527					
000128	000150 74 13 12 12 0 000000					
000129	000151 27 02 14 13 0 000002					
000130	000152 06 01 14 00 0 000067					
000131	000153 27 01 15 13 0 000002					
000132	000154 74 13 12 12 0 000000					
000133	000155 05 00 00 00 0 000014					
000134	000156 02 00 00 00 0 000070					
000135	000157 74 13 12 12 0 000000					
000136	000160 27 16 14 00 0 000003					
000137	000161 74 13 12 12 0 000000					
000138	000162 27 16 14 00 0 000561					
000139	000163 74 13 12 12 0 000000					
000140						
000141						
000142						
000143						
000144						
000145						
000146						
000147						
000148						
000149						
000150						
000151						
000152						
000153						
000154						
000155						



000156	000144	25 00 15 00 0 000014	AN	A1,A0	• A0=LOW CORE ADDRESS A1= UPPER
000157	000145	24 14 15 00 0 000017	A,14	A1,36+35	• DEVELOP CORE RANGE / 36 (BITS)
000158	000146	73 03 01 00 0 000044	DSL	A1,36	• COVERED QUOTIENT+1
000159	000147	34 16 01 00 0 000044	DT,14	A1,36	• CREATE BIN LENGTH IN A1
000160	000148	27 02 14 13 0 000002	L,2	AU,2,B11	• INITIALIZE
000161	000149	06 01 14 00 0 000577	S,1	AU,TRP1	
000162	000150	20-35 +CC 1			
000163	000151	06 01 14 00 0 000600	S,1	AU,TRP2	
000164	000152	20-35 +CC 1			
000165	000153	06 01 14 00 0 000571	S,1	AU,TRP3	
000166	000154	20-35 +CC 1			
000167	000155	74 13 12 12 0 000000	L,14	B10,B10	
000168	000156	74 13 12 12 0 000000	LMJ	B10,B10	
000169	000157	06 00 13 00 0 000043	• LMJ	B11,TRCX\$	• DISABLE ANY TRACE ROUTINE
000170	000158	20-35 +CC 0	S	B11,TRSB11	• LMJ USUALLY WAS UNDER TRACE
000171	000159	74 13 13 00 0 001010	LMJ	B11,PREA\$	
000172	000160	000000 000003	+	0,MTTRCS	
000173	000161	27 00 13 00 0 000043	L	B11,TRSB11	• SET B11 TO AID USEK DEBUG
000174	000162	20-35 +CC 0			
000175	000163	74 04 00 13 0 000000	J	B11	
000176	000164	24 16 13 00 0 000001	A,14	B11,1	• BYPASS NOP S LINE OF FOR IV
000177	000165	74 04 00 00 0 000176	J	TRCX\$	
000178	000166	20-35 +CC 1			• FOR IV CALL NTRC(I,M,SX,SY,NBIN,L)
000179	000167	06 00 13 00 0 000043	S	B11,TRSB11	
000180	000168	20-35 +CC 0			
000181	000169	06 00 12 00 0 000042	S	B10,TRSB10	
000182	000170	20-35 +CC 0			
000183	000171	72 01 00 00 0 000066	SLJ	TAPAK	• INTERRUPT ROUTINE NUMBER
000184	000172	20-35 +CC 1			• TEST FOR STD. ROUTINE
000185	000173	27 00 14 13 1 000800	L	AU,0,B11	• ILLEGAL SWITCH
000186	000174	54 16 00 00 0 000004	TL,14	AU,TRVE-TRV+1	• GET INTERRUPT INITIALIZATION ADDRESS
000187	000175	54 16 00 00 0 000001	TL,14	AU,1	• USE LINK1 TO BYPASS IT
000188	000176	05 00 00 00 0 000014	SZ	AU	• NO. PARAM LINES+ NOP LINE
000189	000177	27 01 14 14 0 000021	L,1	AU,TRV,40	
000190	000178	20-35 +CC 0			
000191	000179	06 01 13 12 14 0 000000	LMJ	B10,AN	• GIMMICK TRNPAR REFERENCING
000192	000180	27 16 14 00 0 000007	L,14	AU,7	• CONTINUE WITH TRCS LINK2
000193	000181	72 01 00 00 0 000046	SLJ	TRCFTA	• COUNT FORIV NOP LINE AS 1 PARAM
000194	000182	20-35 +CC 1			
000195	000183	27 16 13 00 0 000064	L,14	B11,TRNPAR	• NO PARAMS BELOW SLII CALL
000196	000184	20-35 +CC 1			• SET UP ERROR EXIT AND RETURN LINE
000197	000185	74 04 00 00 0 000115	J	TRCL2	
		20-35 +CC 1			
		27 16 14 00 0 000001	NTNCR	AU,1	
		74 04 00 00 0 000225	J	TRCPS1	
		20-35 +CC 1			
		05 00 00 00 0 000014	TRCPS*	AU	
		72 01 00 00 0 000046	SLJ	TRCFTA	
		20-35 +CC 1			
		06 00 13 00 0 000043	S	B11,TRSB11	

000198	000227	27 01 14 00 0 000411	L+1	AU+TRIC	
000199	000230	27 01 14 00 0 000411	TALE+14	AU+TRIC	
000200	000231	27 01 14 00 0 000411	J	INCERR	• TEST FOR INITIALIZED INTERRUPT ROUTINE
000201	000232	27 01 14 00 0 000411	S	000+TRSB10	• NO INTERRUPT NAME = NO PRIOR TRACE
000202	000233	27 01 14 00 0 000411	J	INC44	• TAKE LINK 4 AS RE-ENTRY POINT
000203					
000204					
000205					
000206					
000207					
000208	000234	27 01 14 00 0 000411	S+1	AU+TRSV1	• SOFTWARE HEART OF TRACE ROUTINE
000209	000235	27 01 14 00 0 000411	S+1	AU+TRSV1	• ASSUMES AU IS ADDRESS NSI+TRSAU CONTAINS SAVED AU, TRACE DISENGAGED
000210	000236	27 01 14 00 0 000411	L	AU+TRSV1	• INITIALIZE SKIP SWITCH
000211	000237	27 01 14 00 0 000411	SSL	AU+TRSV1	• SET UP NEXT ADDRESS
000212	000238	27 01 14 00 0 000411	PAIJ	AU+TRSV1	• BRING NEXT INSTRUCTION
000213	000239	27 01 14 00 0 000411	S	PLC+TRSR3	• SHIFT FOR FUNCTION CODE
000214	000240	27 01 14 00 0 000411	TE+14	AU+TRSV1	• AVOID TRACING PARASITES
000215	000241	27 01 14 00 0 000411	TALE+14	AU+TRSV1	• AND I/O INTERRUPT BETWEEN ETMJ AND JUMP
000216	000242	27 01 14 00 0 000411	J	SLJLKV	• SAVE P3 FROM TRACE DESTRUCTION
000217	000243	27 01 14 00 0 000411	TE+14	AU+TRSV1	• LMJ OP CODE
000218	000244	27 01 14 00 0 000411	TALE+14	AU+TRSV1	• SLJ OP CODE
000219	000245	27 01 14 00 0 000411	J	TRPAJ	• AAJ OP CODE
000220	000246	27 01 14 00 0 000411	TALE+14	AU+TRSV1	• PAIJ OR AAJ OP CODE
000221	000247	27 01 14 00 0 000411	J	TRPAJ	• EX OP CODE
000222	000248	27 01 14 00 0 000411	TALE+14	AU+TRSV1	• CAUTION ON EX CHAIN
000223	000249	27 01 14 00 0 000411	L	AU+TRSA0	• ENGAGE TRACE FOR POSSIBLE JUMP NEXT
000224	000250	27 01 14 00 0 000411	ETMJ	TRKX	• *** TRACE MONITOR ***
000225	000251	27 01 14 00 0 000411	EX	FILL	• SHOW NO SKIP
000226	000252	27 01 14 00 0 000411	SZ+1	TRSW1	• K3 COULD CHANGE FROM STORE, LOAD,
000227	000253	27 01 14 00 0 000411	S	K3+TRSR3	• LR REPEATED SEQUENCE
000228	000254	27 01 14 00 0 000411	TALE+1	TRSW1	• NO SKIP ( THIS JUMP TRACED )
000229	000255	27 01 14 00 0 000411	J	TRNSKP	• SKIP OCCURED (THIS JUMP TRACED )
000230	000256	27 01 14 00 0 000411	J	TRNSYP	
000231	000257	27 01 14 00 0 000411			
000232	000258	27 01 14 00 0 000411			
000233	000259	27 01 14 00 0 000411			
000234	000260	27 01 14 00 0 000411			

000235	27 00 14 00 0 000035	SLJLMJ	L	AU*TRSA0	
000236	* 20-35 +CC 0				• EXECUTE WITHIN EXTERNAL PROGRAM
000237	72 12 00 00 1 000254	ETMJ		*TRFX	
000238	* 20-35 +CC 1				• AAIJ OP CODE
000239	000244 52 16 00 00 0 001653	TRPAJ	TE+14	AU*NI653	
000240	000245 74 04 00 00 0 000270		J	TRAAIJ	
000241	* 20-35 +CC 1				• SET SW TO PREVENT I/O ENABLE AFTER
000242	000246 05 02 00 00 0 000074	TPPAIJ	SZ+2	TKSW1	
000243	* 20-35 +CC 0				• A TRACED PAIJ INSTRUCTION
000244	000247 74 04 00 00 0 000262		J	TRC2	• AGT PAIJ INSTRUCTION IN SITU FOR SPEED
000245	* 20-35 +CC 1				• SET SW TO ALLOW I/O AFTER K3 RESTORE
000246	000270 06 02 14 00 0 000074	TRAAIJ	S+2	AU*TRSM1	
000247	* 20-35 +CC 0				• GET AAIJ B+H+I+U
000248	000271 27 00 14 00 1 000254		L	AU*STREX	
000249	* 20-35 +CC 1				• SAVE BHIU
000250	000272 06 00 14 00 0 000075		S	AU*TRBHIU	
000251	* 20-35 +CC 0				
000252	000273 27 00 14 00 0 000035		L	AU*TRSA0	
000253	* 20-35 +CC 0				• ALLOW TO BRING CONTROL BACK TO TRACE
000254	000274 72 12 00 00 0 000275		ETMJ	S+1	
	* 20-35 +CC 1				• USE BHIU WITHOUT AAIJ
	000275 74 04 00 00 1 000075		J	*TRBHIU	
	* 20-35 +CC 0				• TREX HAS FROM ADDRESS OF AAIJ
	000276 27 00 14 00 1 000254	TRAN	L	AU*STREX	• TRACE ROUTINE THINKS JUMP CAME FROM
	* 20-35 +CC 1				• EXTERNAL PROGRAM
	000277 06 00 14 00 0 000075		S	AU*TRBHIU	• GET EX BHIU
	* 20-35 +CC 0				• SAVE BHIU
	000300 27 00 14 00 0 000035		L	AU*TRSA0	• (FILM COMPLETELY RESTORED)
	* 20-35 +CC 0				
	000301 06 00 01 00 0 000044		I	DO	• SAVE B1-B15+44
	* 20-35 +CC 0				
	000302 06 00 02 00 0 000045				
	* 20-35 +CC 0				
	000303 06 00 03 00 0 000046				
	* 20-35 +CC 0				
	000304 06 00 04 00 0 000047				
	* 20-35 +CC 0				
	000305 06 00 05 00 0 000050				
	* 20-35 +CC 0				
	000306 06 00 06 00 0 000051				
	* 20-35 +CC 0				
	000307 06 00 07 00 0 000052				
	* 20-35 +CC 0				
	000310 06 00 10 00 0 000053				
	* 20-35 +CC 0				
	000311 06 00 11 00 0 000054				
	* 20-35 +CC 0				
	000312 06 00 12 00 0 000055				
	* 20-35 +CC 0				
	000313 06 00 13 00 0 000056				
	* 20-35 +CC 0				



```

000351 * <0-35>+CC 0 000060
000352 * <0-35>+CC 0 000061
000353 * <0-35>+CC 0 000062
000354 * <0-35>+CC 0 000063
000355 * <0-35>+CC 0 000064
000356 * <0-35>+CC 1 000065

000356 74 04 00 00 0000356
000357 * <0-35>+CC 1 0000357
000358 * <0-35>+CC 0 0000358
000359 * <0-35>+CC 0 0000359
000360 50 02 00 00 0000360
000361 * <0-35>+CC 0 0000361
000362 * <0-35>+CC 1 0000362
000363 * <0-35>+CC 0 0000363
000364 * <0-35>+CC 0 0000364
000365 * <0-35>+CC 0 0000365
000366 * <0-35>+CC 0 0000366
000367 * <0-35>+CC 0 0000367
000368 * <0-35>+CC 1 0000368
000369 * <0-35>+CC 1 0000369
000370 * <0-35>+CC 1 0000370
000371 * <0-35>+CC 1 0000371
000372 * <0-35>+CC 1 0000372

000373 52 16 01 00 0000373
000374 53 16 01 00 0000374
000375 74 04 00 00 0000375
000376 * <0-35>+CC 1 0000376
000377 * <0-35>+CC 0 0000377
000378 * <0-35>+CC 0 0000378
000379 * <0-35>+CC 0 0000379
000380 25 16 15 00 0000380
000381 20 16 01 00 0000381
000382 74 04 00 00 0000382
000383 * <0-35>+CC 0 0000383
000384 * <0-35>+CC 0 0000384
000385 27 01 15 00 0000385
000386 * <0-35>+CC 0 0000386

000269 000270 000271 000272 000273 000274 000275 000276 000277 000278 000279 000280 000281 000282 000283 000284 000285 000286 000287 000288 000289 000290 000291 000292 000293 000294 000295 000296 000297 000298

* RESUME OP CODE TEST ON LAST NEST INSTR.

/
* HARDWARE HEART OF TRACE ROUTINE
* TRACES * IRACED JUMP ENTRANCE JUMP MAY BE IN TRACE ROUTINE ITSELF
* J * S * RETURN LINE
* L * PLC*RRSR3 * RESTORE MLC AFTER TRACE DESTRUCTION
* TZ*2 * TRSW1 * TEST FOR I/O STATE REQUIRED
* AA1J * $+1 * PERFORM REQUIRED AA1J (DELAYED BEFORE)
* S * AU*TRSAU * SAVE A0
* S * AL*TRSA1 * SAVE A1
* L*1 * AL*TRACES * JUMPED 'TO' ADDRESS+1
* AN*14 * AL*1 * CORRECT FOR +1
* S*1 * AL*TRJTO *
* TLE*14 * AL*TRLA+1 * LAST ADDRESS OF TRACE CODE
* TLE*14 * AL*TRFA * FIRST ADDRESS OF TRACE CODE
* J * INXP * JUMP NOT TO TRACE CODE
* J * U*AI *
* TRXP *
* TE*14 * AL*TRSEAS * JUMP IS TO EXTERNAL PROGRAM
* TLE*14 * AL*TRPEAS * WILL MSEA5 CHANGE MITRCS
* J * TRREA * CHECK FOR RESET ERROR ACTION
* L * AU*(1,0) * INTERRUPT LOCATION INDEX
* S * AL*TRSA2 * SAVE A2
* AN*14 * AL*2 * JUMP-TO ADDRESS MINUS 2
* AU*14 * AL*2 * JUMP-TO ADDRESS
* J * TRXP2 * CONTINUE IN ALTERNATE BANK FOR SPEED
* TRAP0 * L*1 * AL*TRJTO

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000335	000401	27 00 15 00 0 000030	L	A1,TRSA1	•
000336	000402	* 20-35 +CC 0	J	*TRJTO	• TAKE J TO MREAS OR MSEAS
000337	000403	* 20-35 +CC 0	S	A3,TRSA3	• APPLY MORE STRINGENT TESTS
000338	000404	* 20-35 +CC 0	L,13	A3,TRILOC-1,1A0	• SET P REGISTER ADJUSTMENT
000339	000405	* 20-35 +CC 0	S,0	A3,PSIP	• FOR ASSUMED ERROR INTERRUPT
000340	000406	* 20-35 +CC 0	L	A3,TRILOC-1,1A0	• GET INTERRUPT INSTR. IN
000341	000407	73 02 03 00 0 000032	SSL	A3,36-10	• GET OP CODE
000342	000408	24 16 15 00 0 000001	A,14	A1,1	• MAKE ADDRESS AN SLJ U-FIELD SHOULD HAVE
000343	000409	53 16 03 00 0 001641	TNL,14	A3,01641	• SLJ OP CODE
000344	000410	53 01 01 14 1 000010	TNL,1	A1,TRILOC-1,1A0	• IF = AN SLJ INTERRUPT INSTR. WAS XQT
000345	000411	* 20-35 +CC 0	J	TRISLJ	• ABOVE TEST ASSUMES HI-FIELDS =0
000346	000412	* 20-35 +CC 1	L,1	A1,TRJTO	• RESTORE JUMP-TO ADDRESS
000347	000413	* 20-35 +CC 0	L	A3,TRSA3	
000348	000414	53 16 02 14 1 000010	TNL,14	A2,TRILOC-1,1A0	
000349	000415	* 20-35 +CC 0	J	TRJUMP	• NON-SLJ JUMP ON INTERRUPT OAS XQT
000350	000416	* 20-35 +CC 1	L	A3,TRSA3	
000351	000417	* 20-35 +CC 0	J	TRXPO	• NO ERROR INTERRUPT ACTUALLY OCCURRED
000352	000418	* 20-35 +CC 1	L	A1,TRILOC-1,1A0	• GET INTERRUPT INSTR.
000353	000419	73 02 01 00 0 000032	SSL	A1,36-10	• GET OP CODE
000354	000420	53 16 01 00 0 001641	TNL,14	A1,01641	• SLJ
000355	000421	74 04 00 00 0 000500	J	TRISLJ	
000356	000422	* 20-35 +CC 1	TNL,14	A1,01713	• LMJ
000357	000423	* 20-35 +CC 0	J	TRILFJ	
000358	000424	* 20-35 +CC 1	TNL,14	A1,01707	• AAIJ TEST FOR INTERRUPT LOCATION
000359	000425	* 20-35 +CC 0	J	TRILFJ	
000360	000426	52 16 01 00 0 001653	TE,14	A1,01653	• FAIJ TEST FOR INTERRUPT LOCATION
000361	000427	74 04 00 00 0 000517	J	TRILF2	
000362	000428	* 20-35 +CC 1	SZ,2	TRSW1	• CORRECT I/O STATE SWITCH
000363	000429	* 20-35 +CC 0	PAIJ	TRILF2	• RELATED PAIJ ( COULD BE TOO LAIE)
000364	000430	* 20-35 +CC 1	S,4	A1,TRSW1	• CORRECT I/O STATE SWITCH
000365	000431	* 20-35 +CC 0	AAIJ	TRILF2	
000366	000432	* 20-35 +CC 1	L,1	A1,TRILOC-1,1A0	• GET SLJ'S HIU-FIELDS (ASSUME HI=0)

000367	000501	27 01 14 00 0 000254		L,1	AU,TRXA	• GET CORRECT ERROR ADDRESS
000368	000502	* 20-35 +CC 1		A,0	AU,PSIN	• SIMULATE P REGISTER
000369	000503	* 20-35 +CC 0		S,1	AU,0A1	• STORE 18 CONE OR 36 FILM BITS
000370	000504	06 01 14 15 0 000000		J	TRILP2	• A1=20 OR LESS IS ILLEGAL (SEE LCMCGR)
000371	000505	* 20-35 +CC 1		L	A1,TRILP2	• GET LMJ INSTR.
000372	000506	27 00 15 14 1 000010	TRILP2	SSL	A1,26	• GET A-FIELD OF LMJ
000373	000507	* 20-35 +CC 0		SSL	A1,22	
000374	000508	73 00 01 00 0 000032		TE,14	A1,00	
000375	000509	52 16 01 00 0 000040		TR,14	A1,01	• AU OR A1 IMAGES MUST BE CHANGED
000376	000510	* 20-35 +CC 0		J	TRILP3	• CORRECT 80-811,814,OR 815
000377	000511	74 04 00 00 0 000523		L	AU,0A1	• ERING DOWN CORRECT ERROR ADDRESS
000378	000512	* 20-35 +CC 1		LX,01	AU,TRXA	• SIMULATE P REGISTER
000379	000513	27 00 14 15 0 000000	TRILP3	A,0	AU,PSIN	
000380	000514	* 20-35 +CC 1		S	AU,0A1	
000381	000515	24 10 14 00 0 000016		L,1	A1,TRJTO	
000382	000516	* 20-35 +CC 0		L	A2,TRSA2	
000383	000517	06 00 14 15 0 000000	TRILP4	J	A3,TRSA3	
000384	000518	* 20-35 +CC 0		L,1	TRXP1	• RESUME WITH USER LIMITS TESTS
000385	000519	27 00 16 00 0 000037		L	AU,TRXA	• ERING DOWN CORRECT ADDRESS
000386	000520	* 20-35 +CC 1		A,0	AU,PSIN	• SIMULATE P REGISTER
000387	000521	27 00 17 00 0 000040	TRILP5	EX	TRILP4-AU,0A1	• CHANGE AU OR A1 IMAGE
000388	000522	* 20-35 +CC 0		J	TRILP2	
000389	000523	74 04 00 00 0 000405		L,1		
000390	000524	* 20-35 +CC 1		A,0		
000391	000525	27 01 14 00 0 000254	TRILP6	EX		
000392	000526	* 20-35 +CC 0		J		
000393	000527	24 10 14 00 0 000016		L		
000394	000528	* 20-35 +CC 0		L		
000395	000529	72 10 00 15 0 000003		J		
000396	000530	* 20-35 +CC 1		L		
000397	000531	27 00 15 00 0 000057		SSL		
000398	000532	* 20-35 +CC 0		JSL		
000399	000533	74 04 00 00 0 000517		L		
000400	000534	* 20-35 +CC 0		TR,14		
000401	000535	53 00 00 00 0 000070		J		
000402	000536	* 20-35 +CC 1		SA		
	000537	74 04 00 00 0 000546		SZ		
	000538	* 20-35 +CC 0				
	000539	01 00 00 00 0 000070				
	000540	* 20-35 +CC 0				
	000541	05 00 00 00 0 000071				

THE FOLLOWING ROUTINES ARE THE STD. INTERRUPT ROUTINES

TPCYS\*

• A0=FROM ADDRESS A1=TO ADDRESS

• STORE CYCLIC -- FROM-TO OR REPEAT

• ACCOMMODATE SLJ

• A0=FROM TO PAIR

• NEXT ADDRESS FOR STORAGE

• IS LAST PAIR EQU CURRENT PAIR

• SAVE LAST PAIR

• SET REPEAT COUNT/SWITCH



000403	000577	* 20-35 +CC 0	TRCU1	S	AU+*A1	• STORE IN TRCTBL
000404	000580	25 00 01 00 0 000072	TG	AL+TRTB	• SEE IF END TABLE WILL BE EXCEED	
000405	000581	* 20-35 +CC 0	L	AL+TRTB		
000406	000582	27 00 15 00 0 000073	S	AL+TRNSA		
000407	000583	* 20-35 +CC 0	LN+14	AU+0	• -U	
000408	000584	11 16 00 00 0 000000	S	AU+*A1	• STORE NEG U MARK BETWEEN CYCLES	
000409	000585	06 00 14 15 0 000000	J	TRCVS	• RETURN	
000410	000586	74 04 00 00 0 000527	TZ	TRPA	• IS THIS FIRST EQU FOR PAIR	
000411	000587	* 20-35 +CC 1	J	TREQU1	• NOT FIRST	
000412	000588	27 00 15 00 0 000554	S	AL+TRPA	• SAVE REPEAT ADDRESS	
000413	000589	* 20-35 +CC 1	LN+14	AU+1	• REPEAT COUNT INITIALIZED	
000414	000590	27 16 14 00 0 000001	S+1	AU+*A1	• PRESERVE -0 LEFT HALF FOR REPEAT FLAG	
000415	000591	06 01 14 15 2 000000	J	TRCY1+1		
000416	000592	74 04 00 00 0 000540	L	AL+TRPA		
000417	000593	* 20-35 +CC 1	LN+14	AU+1	• INCREMENT LAST CNT	
000418	000594	27 00 15 00 0 000071	S+1	AU+*A1	• REPEAT MODULUS 2*/18	
000419	000595	* 20-35 +CC 0	J	TRCVS	• LEAVE LEFT HALF A -0 TO FLAG REPEAT	
000420	000596	27 16 14 00 0 000001	J		• RETURN	
000421	000597	06 01 14 15 0 000000				
000422	000598	74 04 00 00 0 000527				
000423	000599	* 20-35 +CC 1				
000424	000600	27 00 15 00 0 000071				
000425	000601	* 20-35 +CC 0				
000426	000602	27 16 14 00 0 000001				
000427	000603	06 01 14 15 0 000000				
000428	000604	74 04 00 00 0 000540				
000429	000605	* 20-35 +CC 1				
000430	000606	27 00 15 00 0 000071				
000431	000607	* 20-35 +CC 0				
000432	000608	27 16 14 00 0 000001				
000433	000609	06 01 14 15 0 000000				
000434	000610	74 04 00 00 0 000540				
000435	000611	* 20-35 +CC 0				
000436	000612	27 00 15 00 0 000071				
000437	000613	* 20-35 +CC 1				

/ TRACED ORIGIN POINT SUBROUTINE TO TRACE		• ANE FROM ADDRESS		A0 AND A1 ARE DESTRUCTIBLE	
TRCPS*	J	S			
000561	TL	AU+TRCUCS			• ACCOMMODATE SLJ
000562	TL	AU+TRCUCS			• UPPER CORE TEST
000563	J	TRCPS			• LOWER CORE TEST
000564	S	A2+TRSA2			• OUTSIDE USERS COME-RETURN
000565	AN+1	AU+TRCUCS			• OBTAIN ADDRESS RELATIVE TO LOWER
000566	DSL	AU+36			
000567	CI+14	AU+76			
000568	LI+4	A2+TRSA3			
000569	TG+1	A2+TRTFE			• TEST TO AVOID TABLE OVERFLOW
000570	J	TRPA			• AVOID
000571	S	A3+TRSA3			
000572	L	A2+1 1*/35			

000438	000076	73 02 01 15 0 000000	TRP1	SSL	A2, A1	• SET BIT FOR TRACED ORIGIN POINT
000439	000077	00 00 02 14 0 177777	TRP2	OR	A2, FILL, A0	• STORE IN TABLE
000440	000080	06 00 17 14 0 177777	TRP4	S	A3, FILL, A0	
000442	000081	27 00 10 00 0 000037		L	A2, TRSA2	
000443	000082	00 00 17 00 0 000040		L	A3, TRSA3	
000444	000083	74 04 00 00 0 000561		J	TRCP3	• RETURN
000445	000084	7777777777	TRP4	-0		• LAST ADDRESS OF TRACE CODE
000446			S(U)	INFO	0 0	• INDEPENDENT TO AVOID OVERLAY
000447			TRAP2	TRAP2	TRAP2	• TEST INTERRUPT LOCATION'S U-FIELD
000448				TRAP2	TRAP2	• AGAINST JUMP-TO ADDRESS RANGE
000449				TRAP2	TRAP2	• MEMORY LOCKOUT
000450				TRAP2	TRAP2	• POSSIBLE ERROR INTERRUPT JUMP
000451				TRAP2	TRAP2	• CHAR. OVERFLOW
000452				TRAP2	TRAP2	• CHAR. UNDERFLOW
000453				TRAP2	TRAP2	• DIVIDE OVERFLOW
000454				TRAP2	TRAP2	• NO ERROR INTERRUPT JUMP XGT
000455				TRAP2	TRAP2	• INDEX 0 ILLEGAL FUNCTION
000456				TRAP2	TRAP2	• INDEX 1 MEMORY LOCKOUT
000457				TRAP2	TRAP2	• INDEX 2 CHAR. UNDERFLOW
000458				TRAP2	TRAP2	• INDEX 3 CHAR. OVERFLOW
000459				TRAP2	TRAP2	• INDEX 4 DIVIDE OVERFLOW
000460				TRAP2	TRAP2	• SIMULATED P REGISTER ADJUSTMENT
000461				TRAP2	TRAP2	• CORRECT THE AN IMAGE
000462				TRAP2	TRAP2	• CORRECT THE A1 IMAGE
000463				TRAP2	TRAP2	• IMPOSSIBLE ADDRESS/SWITCH VALUE
000464				TRAP2	TRAP2	• INTERRUPT CODE SWITCH( ALSO ADDR), SETUP
000465				TRAP2	TRAP2	• INTERRUPT CODE SWITCH( ALSO ADDR), SETUP
000466				TRAP2	TRAP2	
000467				TRAP2	TRAP2	
000468				TRAP2	TRAP2	
000469				TRAP2	TRAP2	
000470				TRAP2	TRAP2	
000471				TRAP2	TRAP2	
000472				TRAP2	TRAP2	
000473				TRAP2	TRAP2	
000474				TRAP2	TRAP2	
000475				TRAP2	TRAP2	

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000032 777777777777  
000033 777777777777  
000034 000000 777777  
000035 000000000000  
000036 000000000000  
000037 000000000000  
000040 000000000000  
000041 000000000000  
000042 000000000000  
000043 000000000000  
000044  
000045 000001 777777  
000046 777777777777  
000047 000000000000  
000048 000001 777777  
000049 000001 777777  
000050 777777777777  
000051 000002000000  
000052 000002000001  
000053 000001 777776  
000054 000001 000000  
000055 000001 000000

K1A  
TPCLC\*  
TPCLC\*  
TPJTO  
TPCAUS\*  
TPSA0  
TPSA1\*  
TPSA1  
TPSA2  
TPSA3  
TPSR3  
TPSR10  
TPSR11  
REG  
TRNPAK  
TRNSA  
TRFLT  
TRRPA  
TRTBE  
TRTES  
TPSV1  
TPSHU  
END

• TRACED ADDM. TO TAKE AS NSI

• TEMP CELLS FOR B1-B15\*44 IF EX CHAIN  
• FOR IV PARAMS PACKED IN SLII CALL SEQ.  
• NEXT CYCLIC TABLE ADDRESS

• 1\*END OF TRC TABLE  
• 1\*START OF TRC TABLE  
• INTERRUPT SWITCH. SKIP SWITCH  
• 0=PREVENT AAIJ  
• UP CODE + DESIRED BHIU BITS OF AAIJ OR  
• NESTED EX INSTRUCTION

10  
3  
1\*FILL  
1\*FILL  
1\*FILL  
1\*0